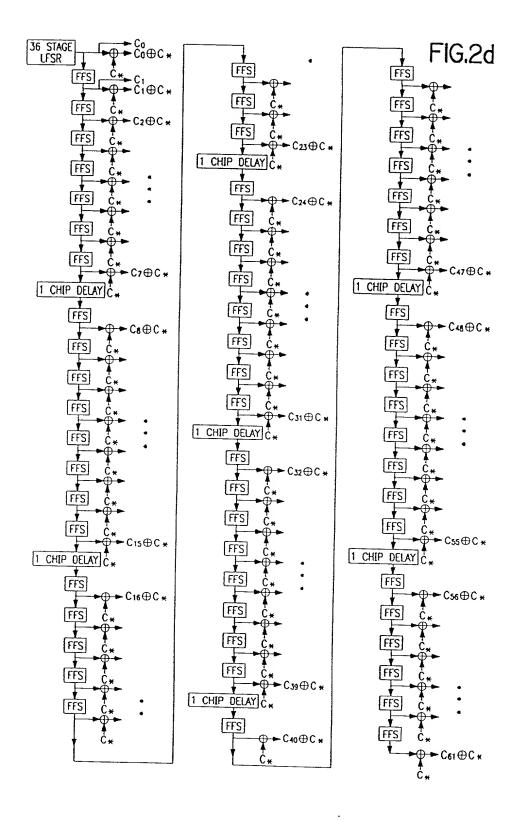


CODE MEMORY



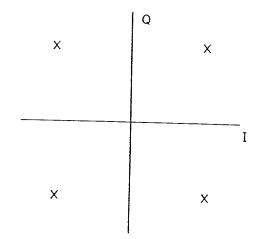


FIG. 3a

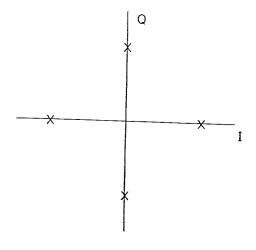
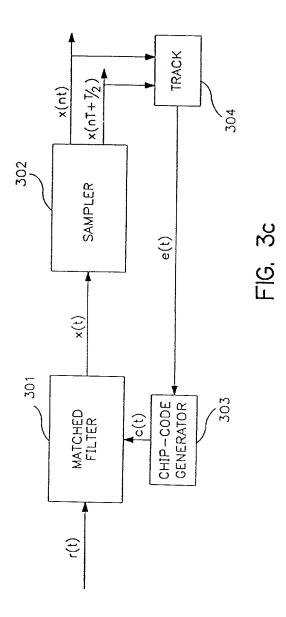
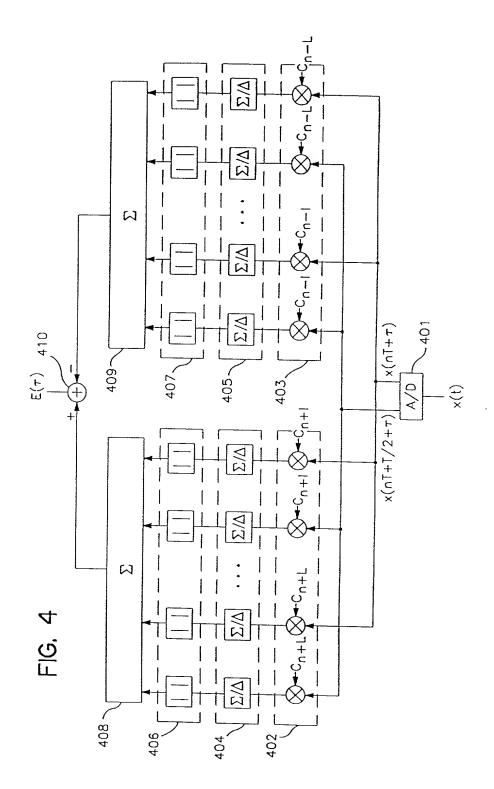


FIG. 3b





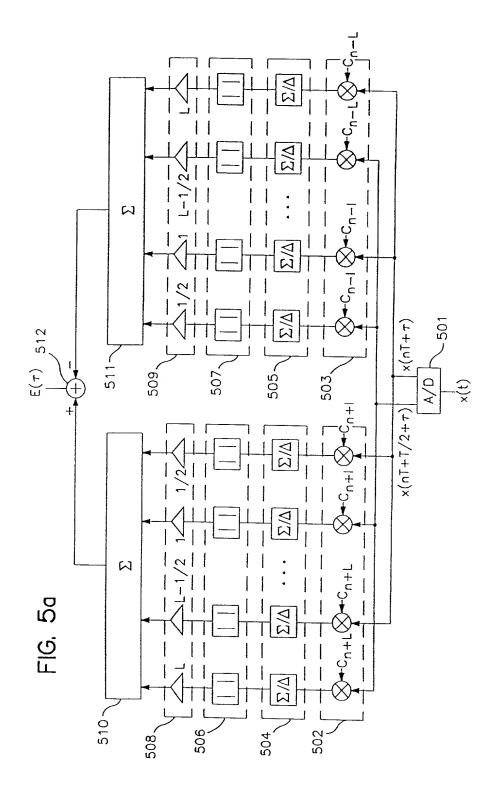
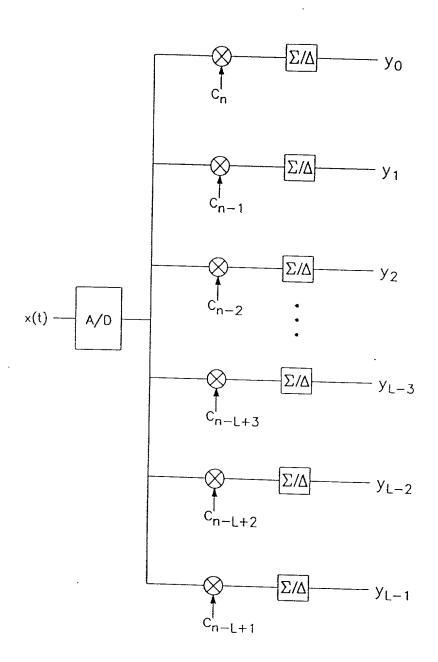


FIG. 5b



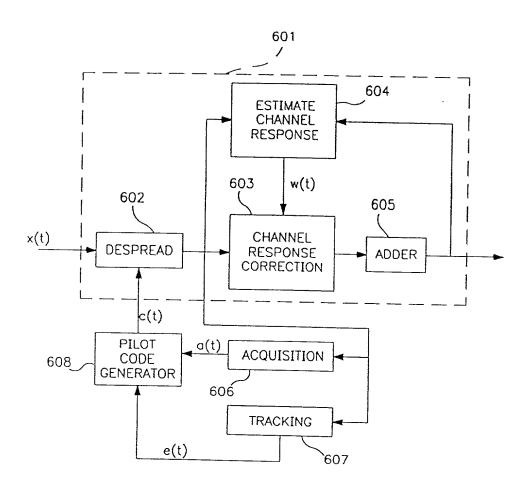
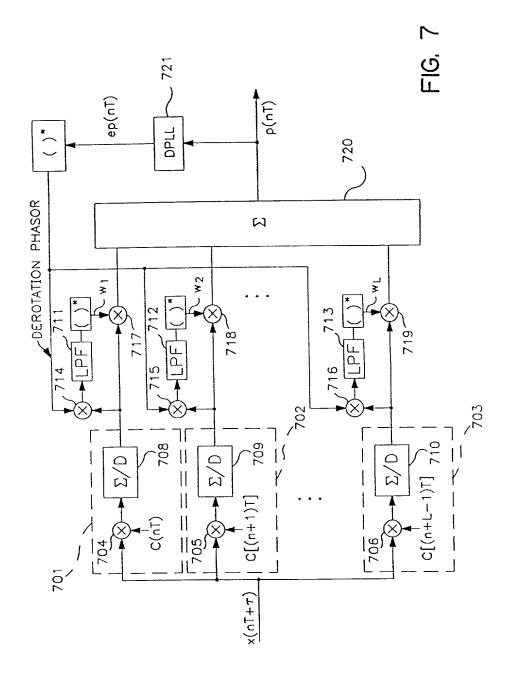


FIG. 6



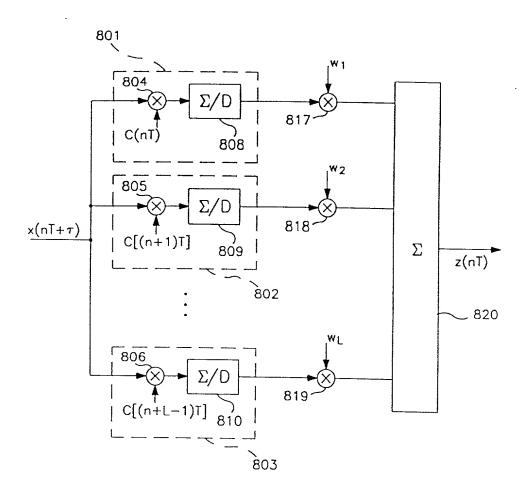


FIG. 8a

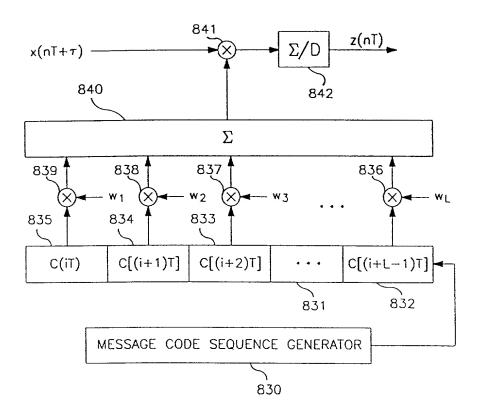
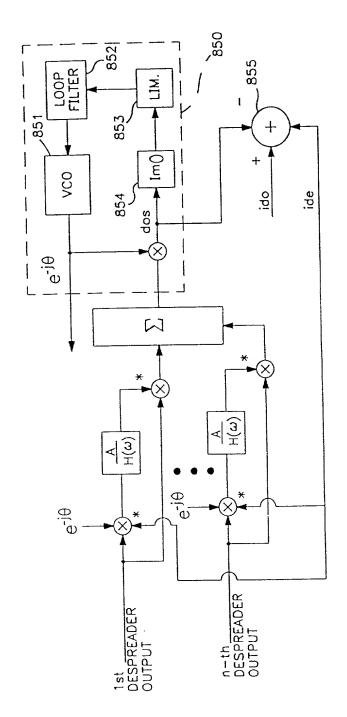
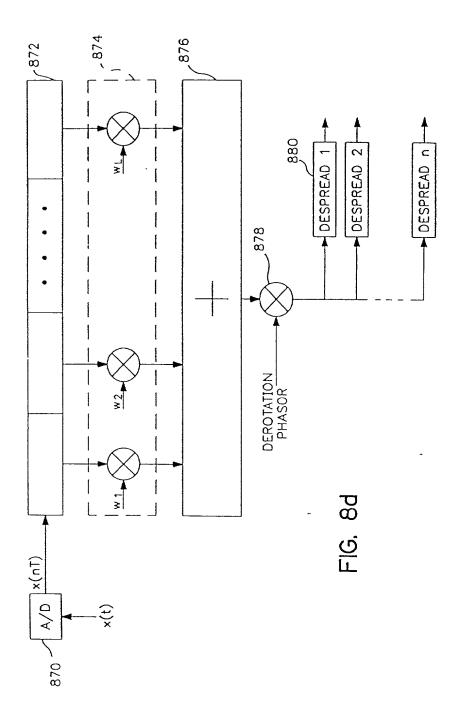
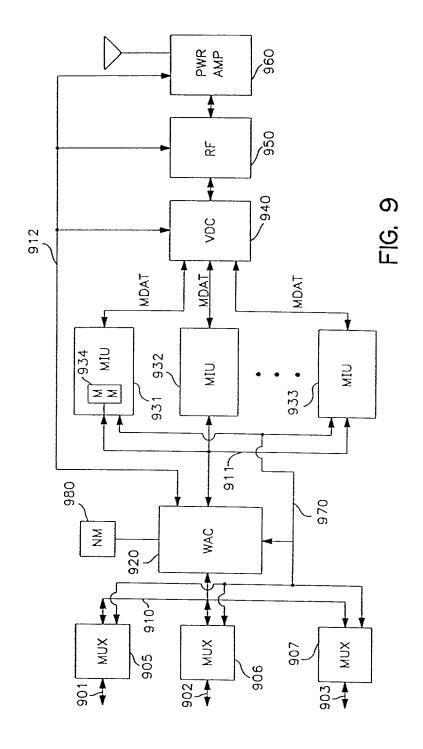


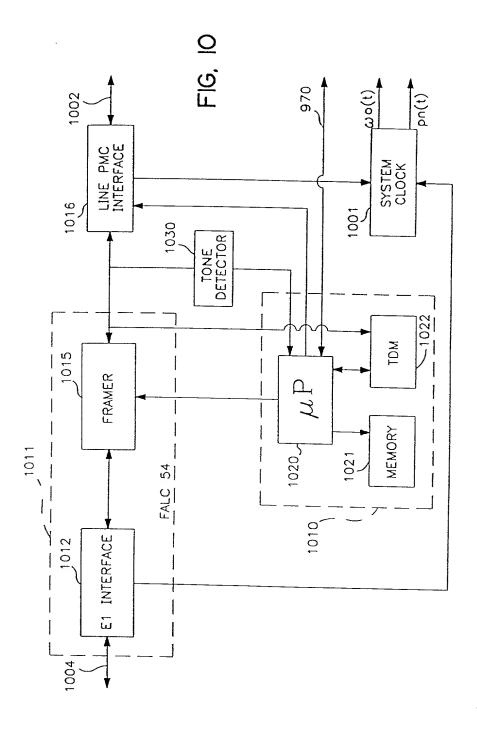
FIG. 8b

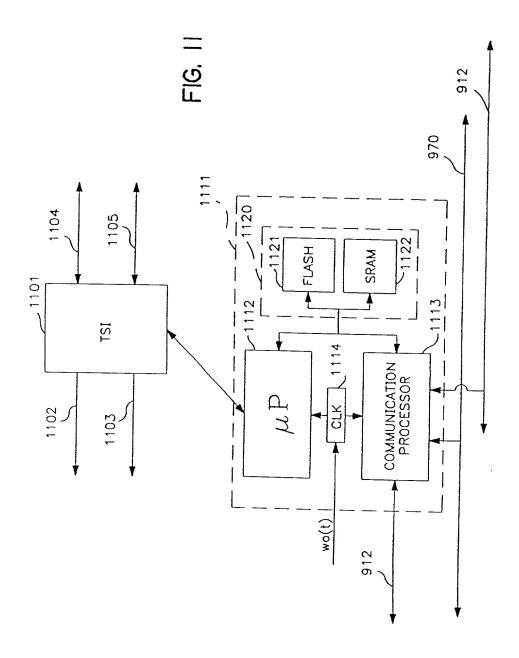


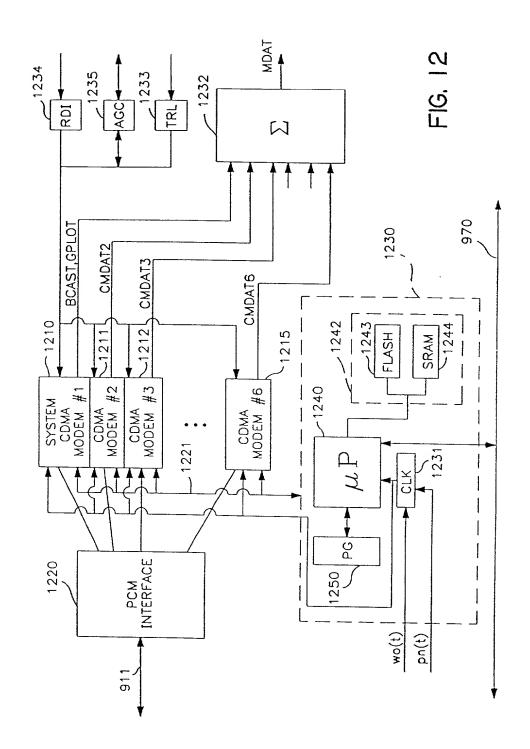
FIG, 8c











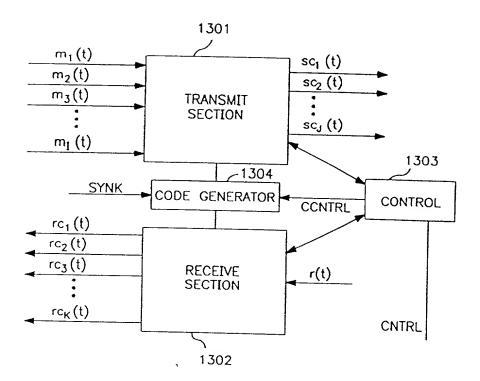
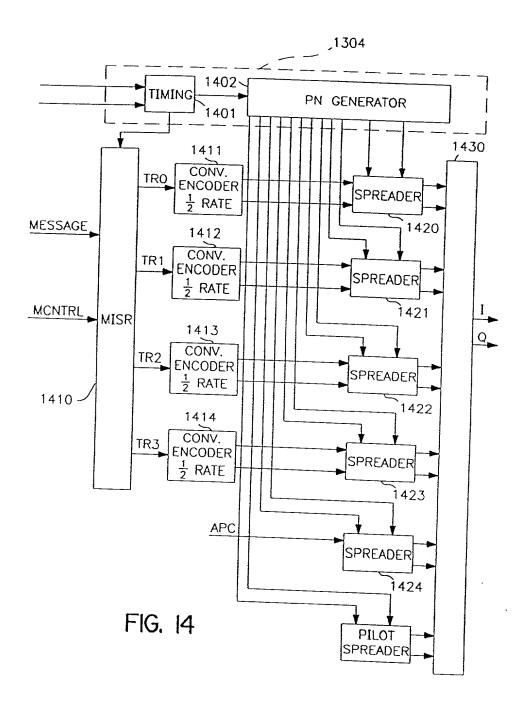
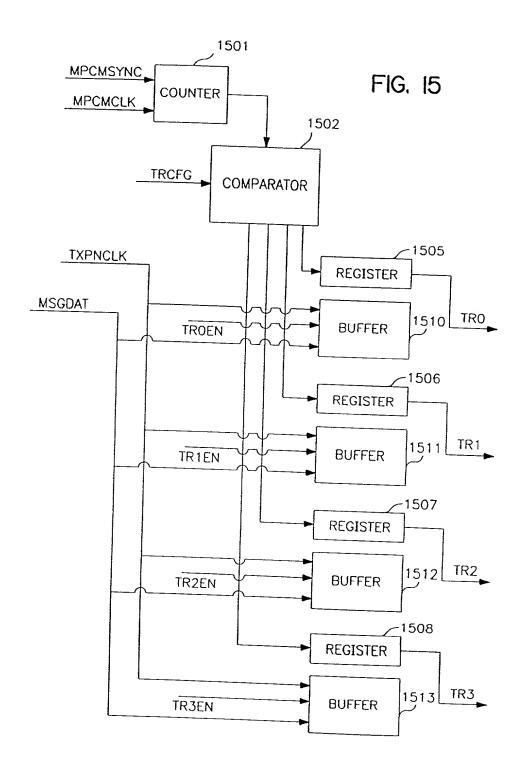


FIG. 13





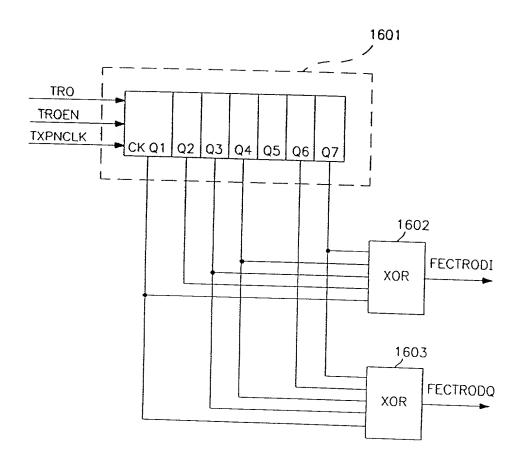


FIG. 16

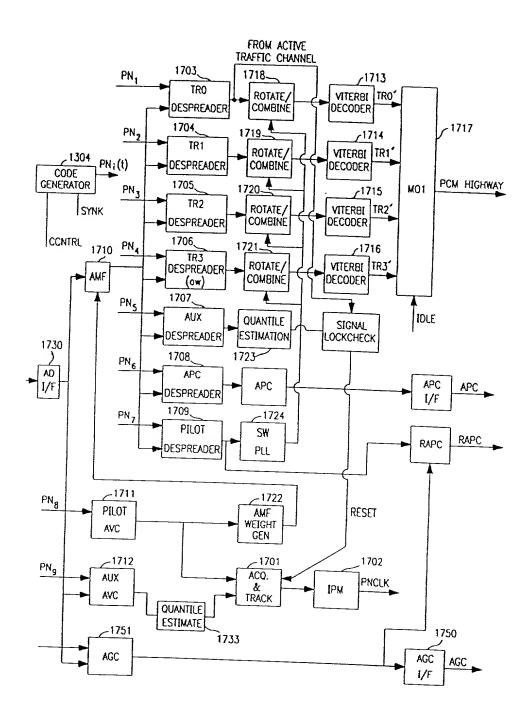
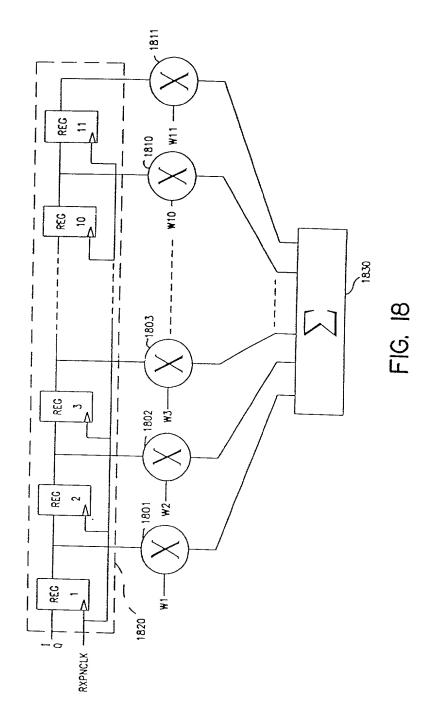
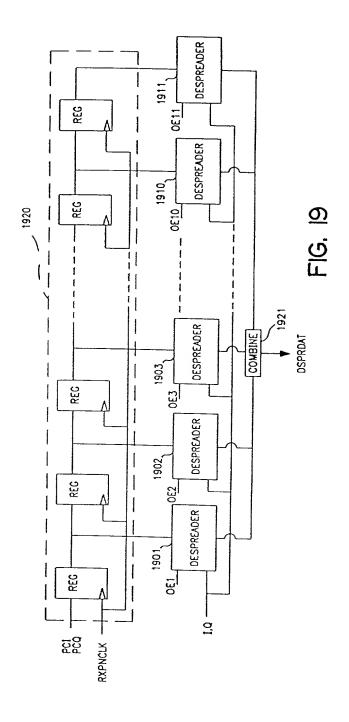
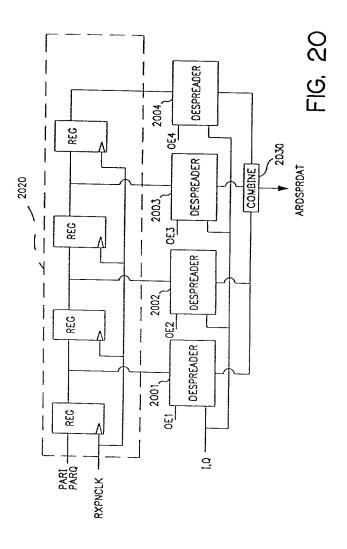
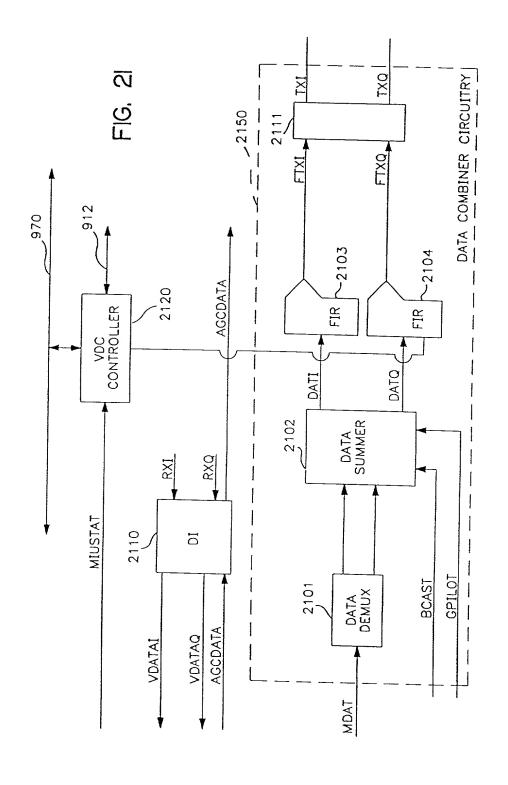


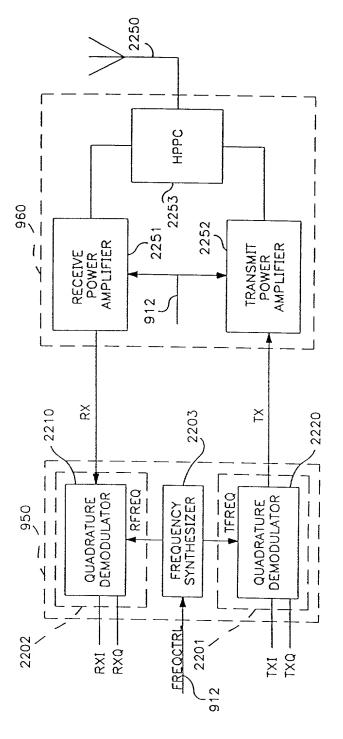
FIG. 17



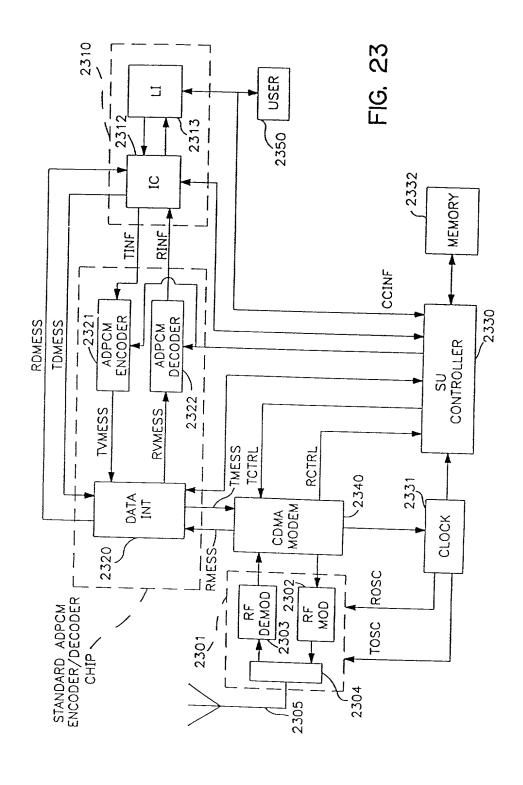


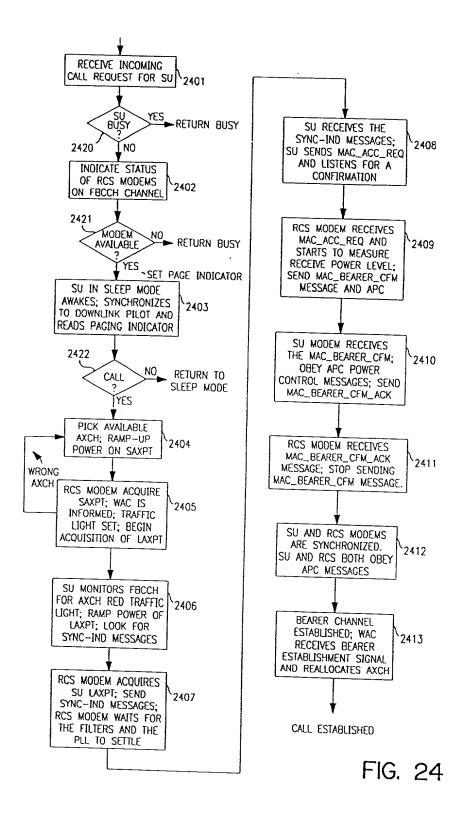


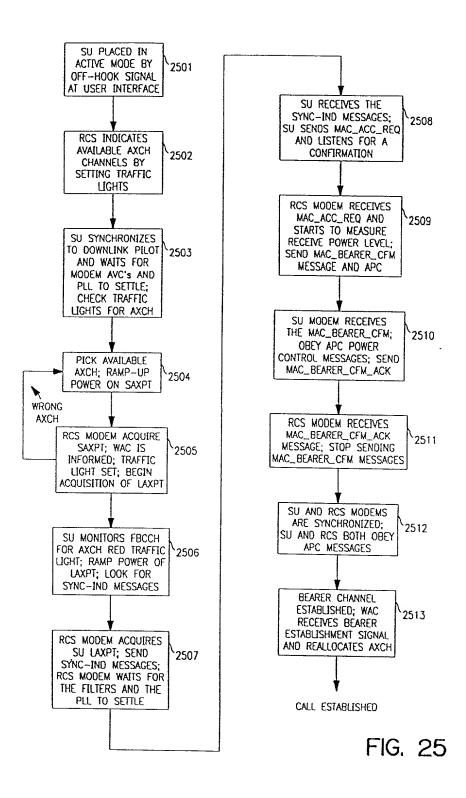




F1G, 22







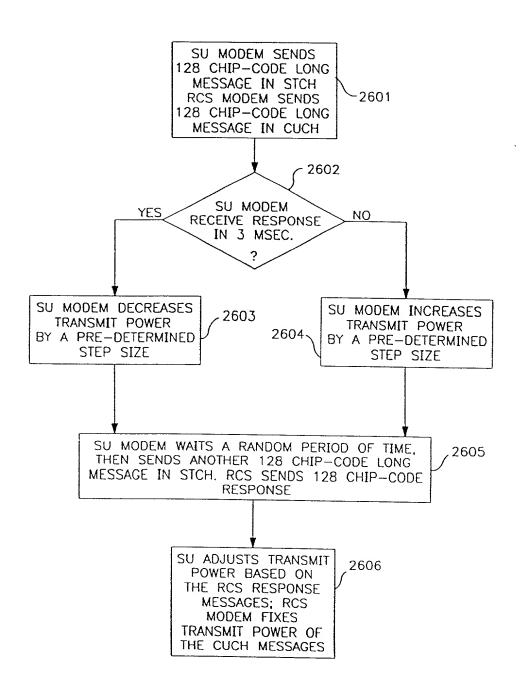


FIG. 26

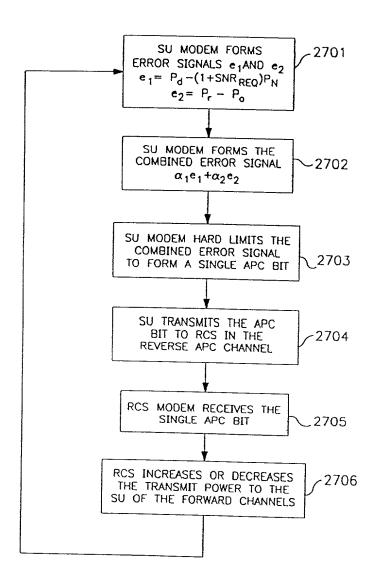


FIG. 27

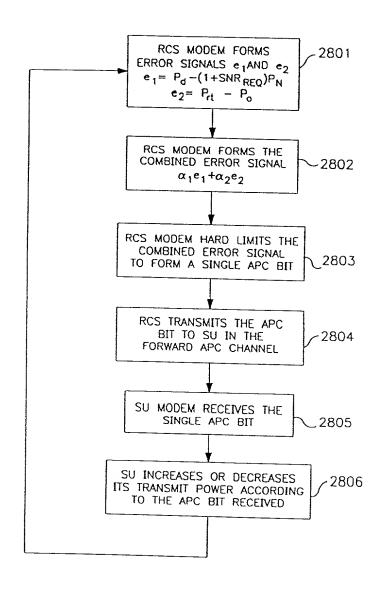
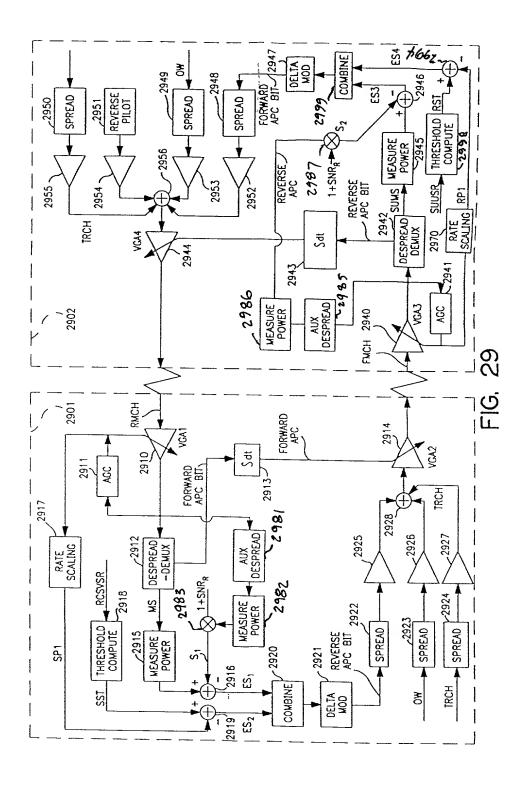


FIG. 28



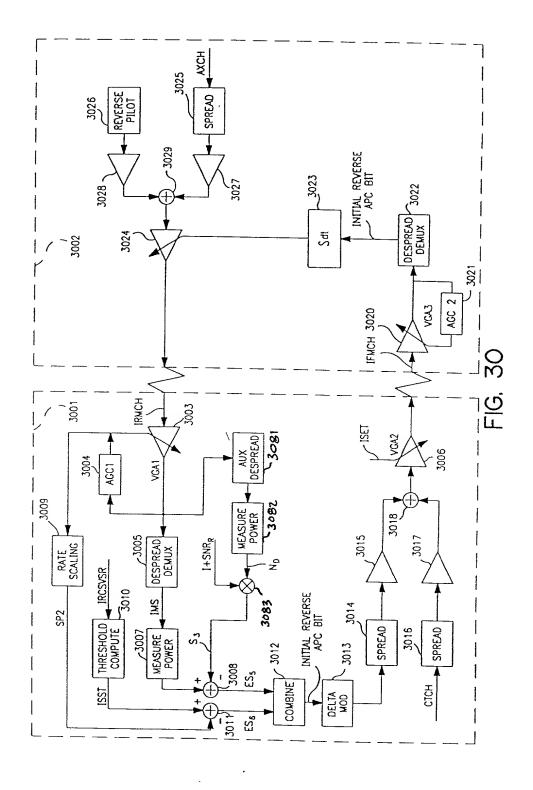


FIG.31

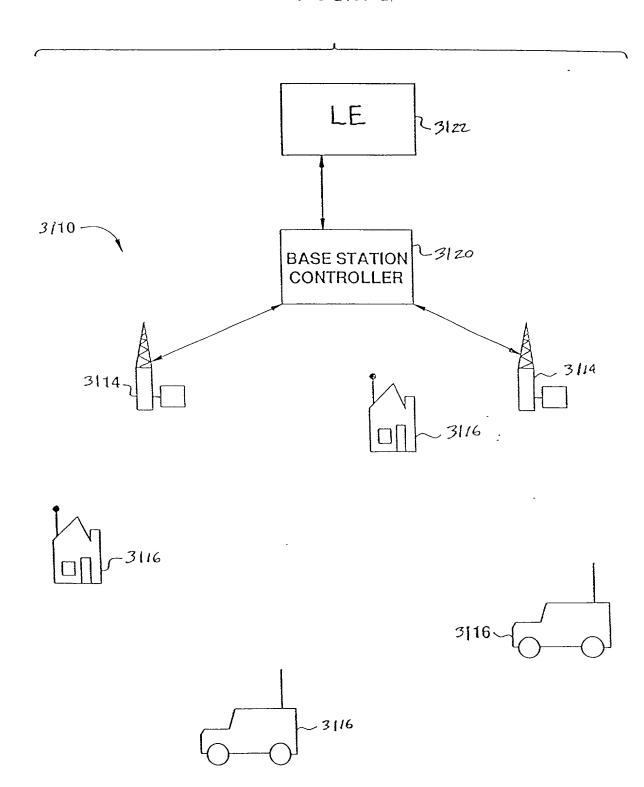
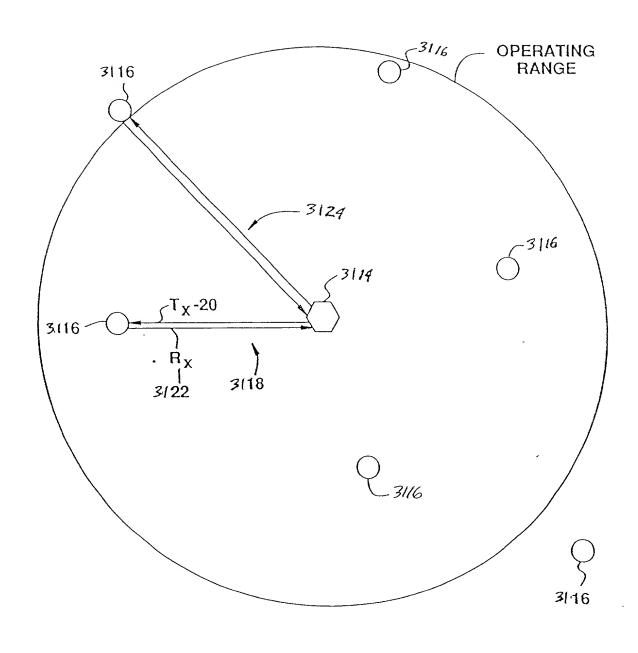


FIG.32



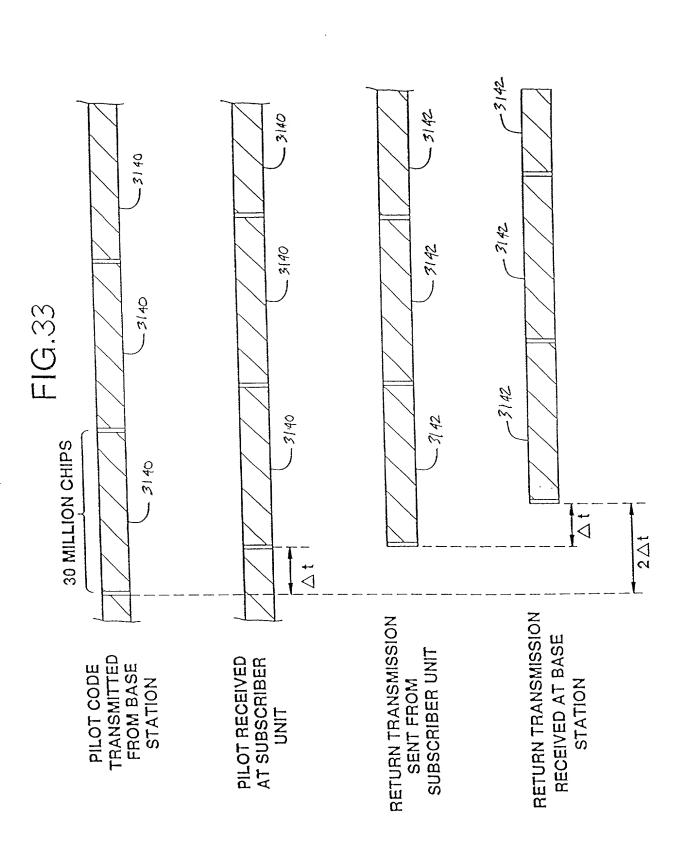


FIG.34

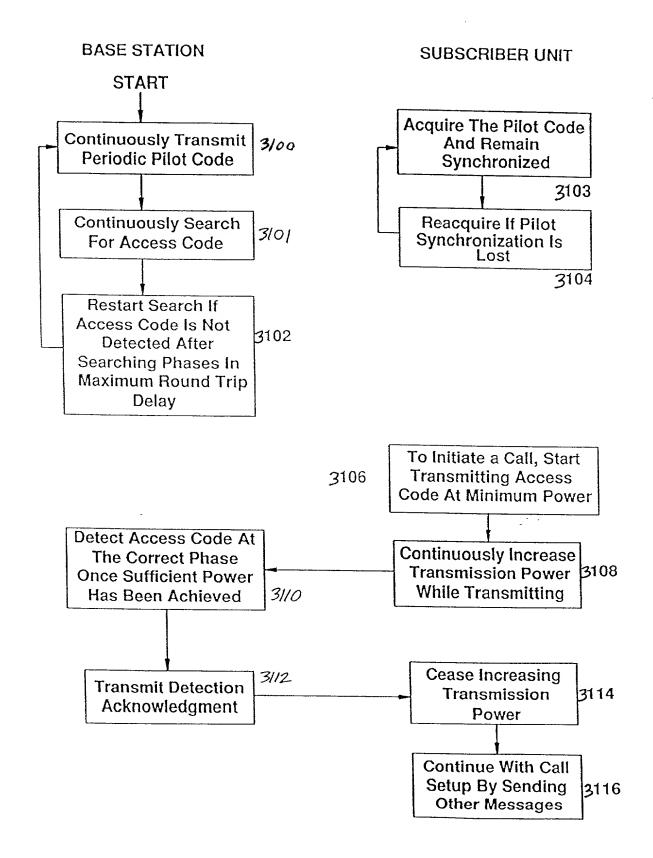


FIG.35

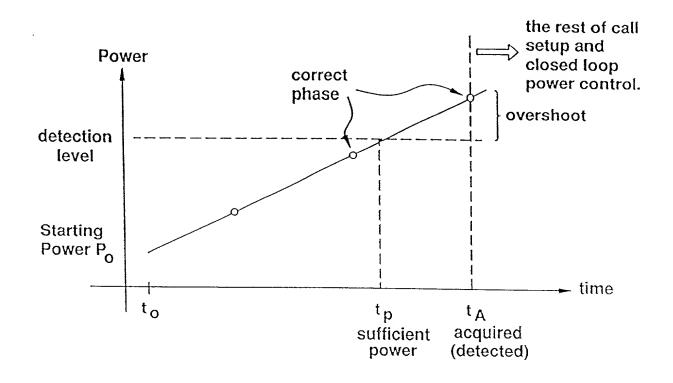


FIG.37

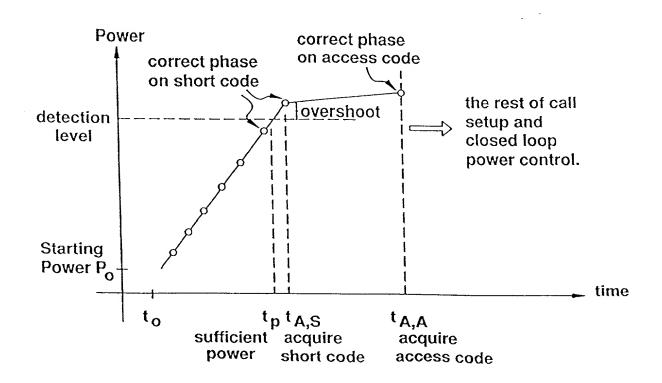


FIG.36A

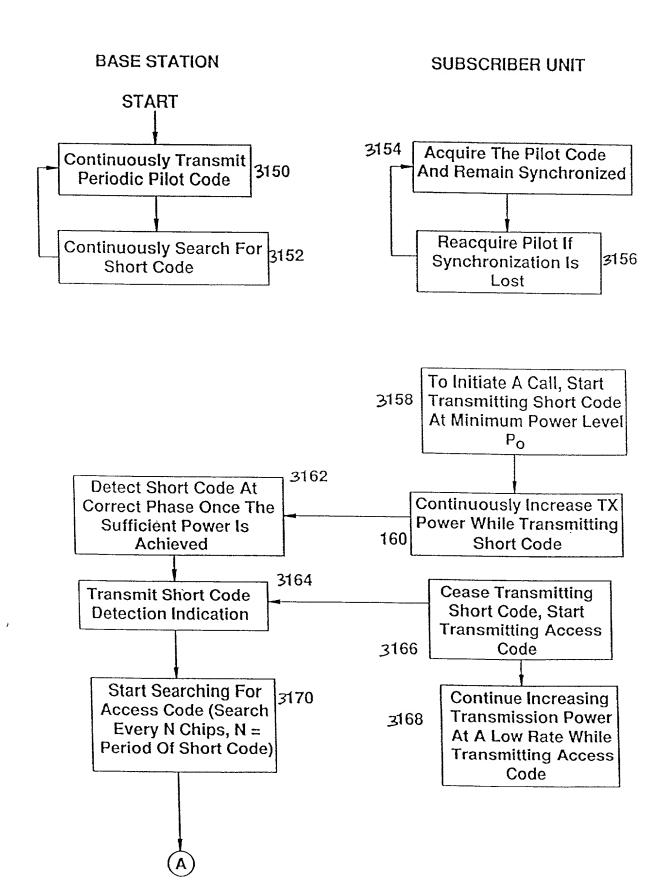


FIG.36B

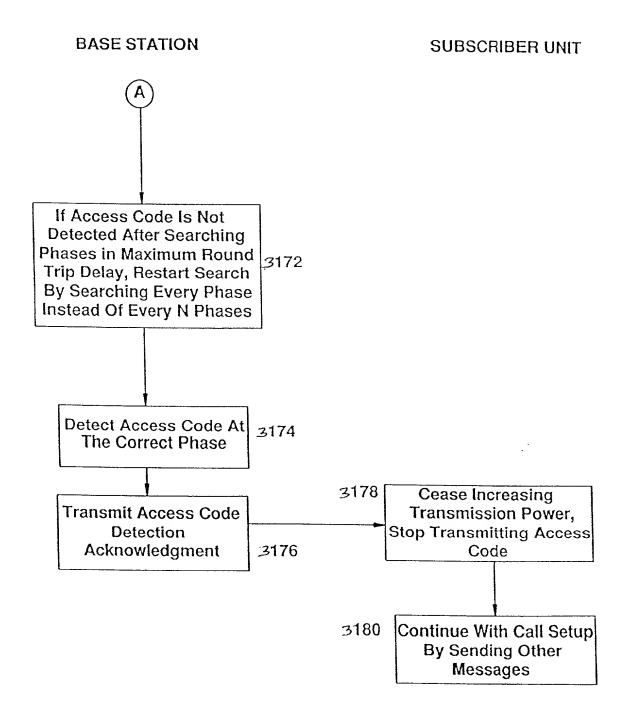
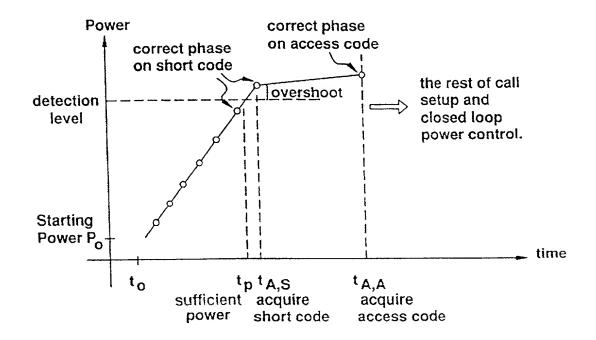
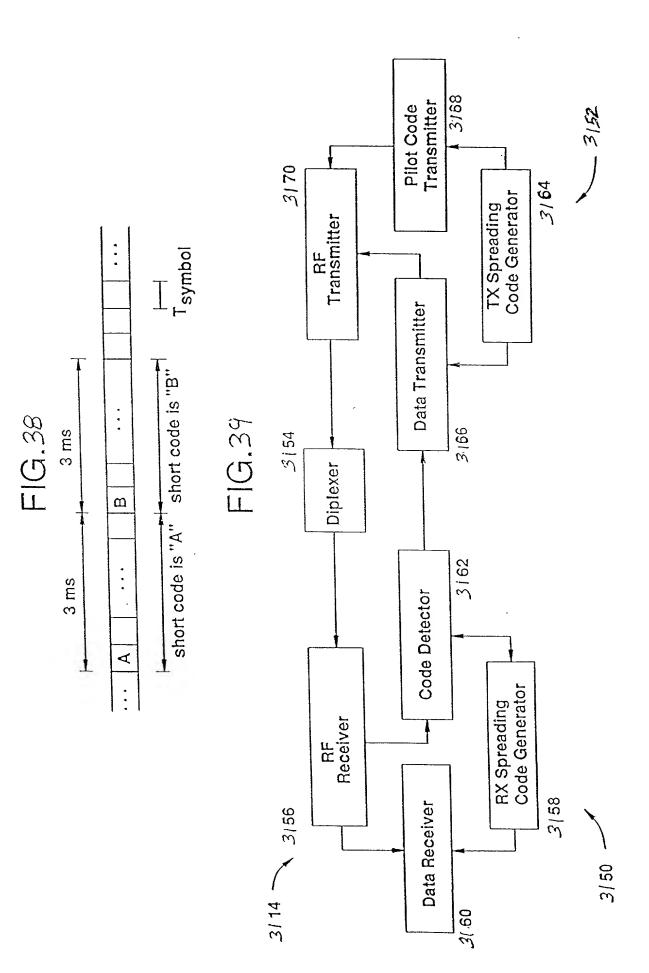


FIG. 37





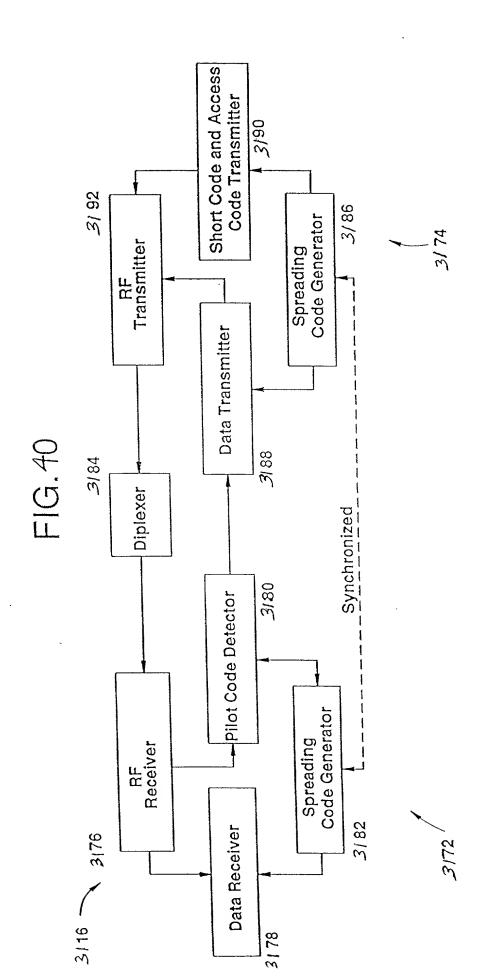


FIG.41A

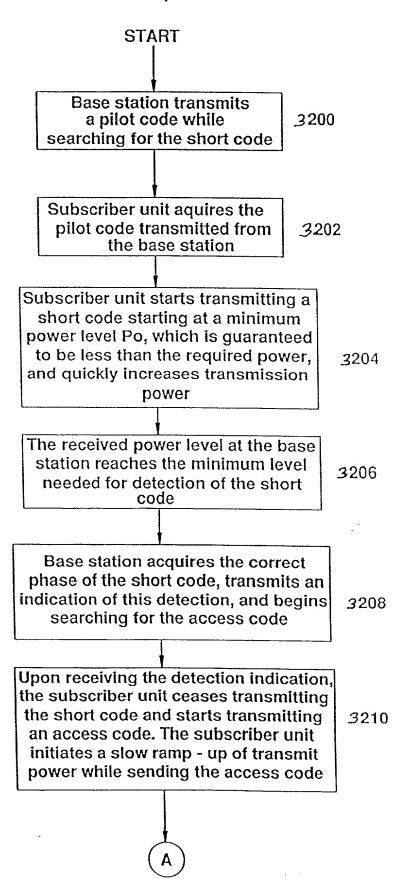


FIG.41B



Base station searches for the correct phase of the acces code by searching only one phase out of each short code length portion of the access code

3212

If the base station searches the phases of the access code up to the maximum round trip delay and has not detected the correct phase, repeat search by searching every phase

3214

Upon detection of the correct phase of the access code by the base station, the base station sends an acknowledgement to the subscriber unit

3216

Reception of the acknowledgement by the subscriber unit concludes the ramp - up process. A closed loop power control is established, and the subscriber unit continues the call setup process by sending releted call setup messages

3218

FIG. 42 (PRIOR ART)

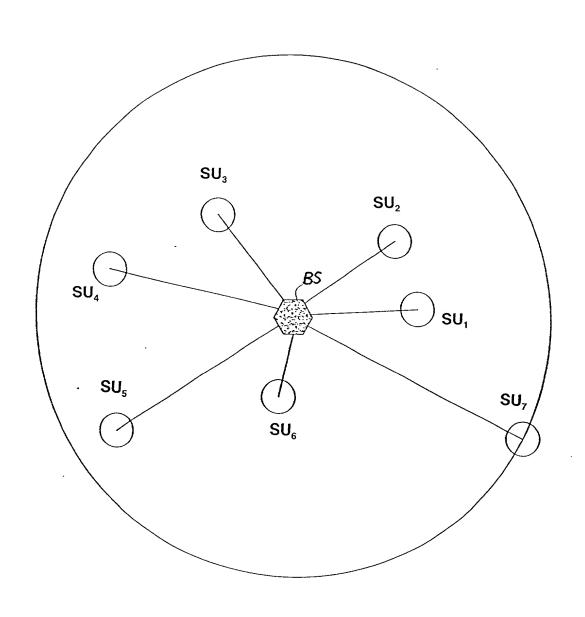
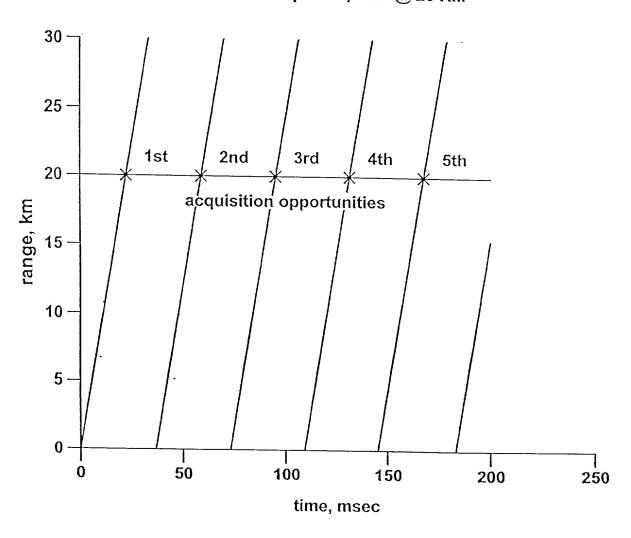


FIG. 43 (PRIOR ART) Mean Cell Sweep Time, FSU @ 20 KM



:

FIG.44

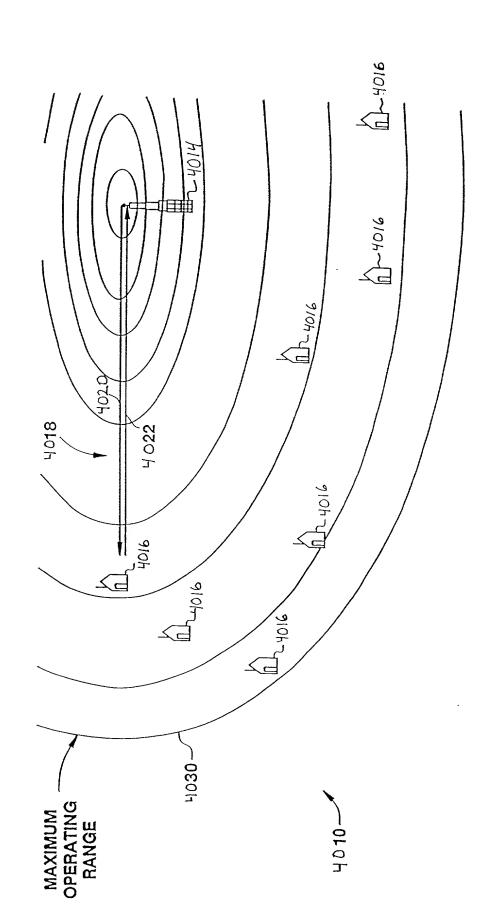


FIG. 45

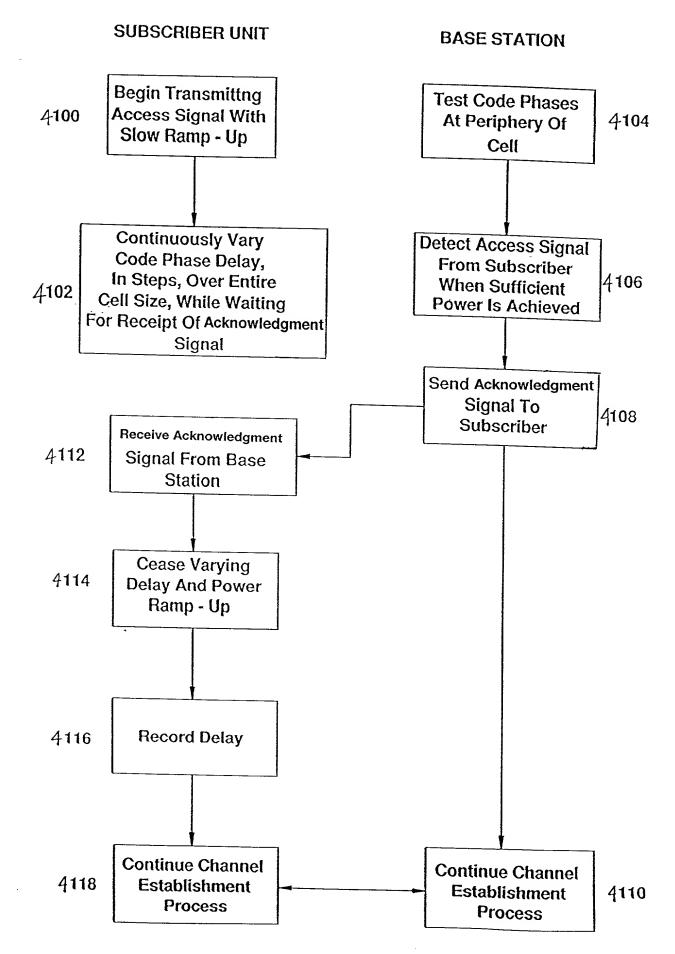


FIG. 46

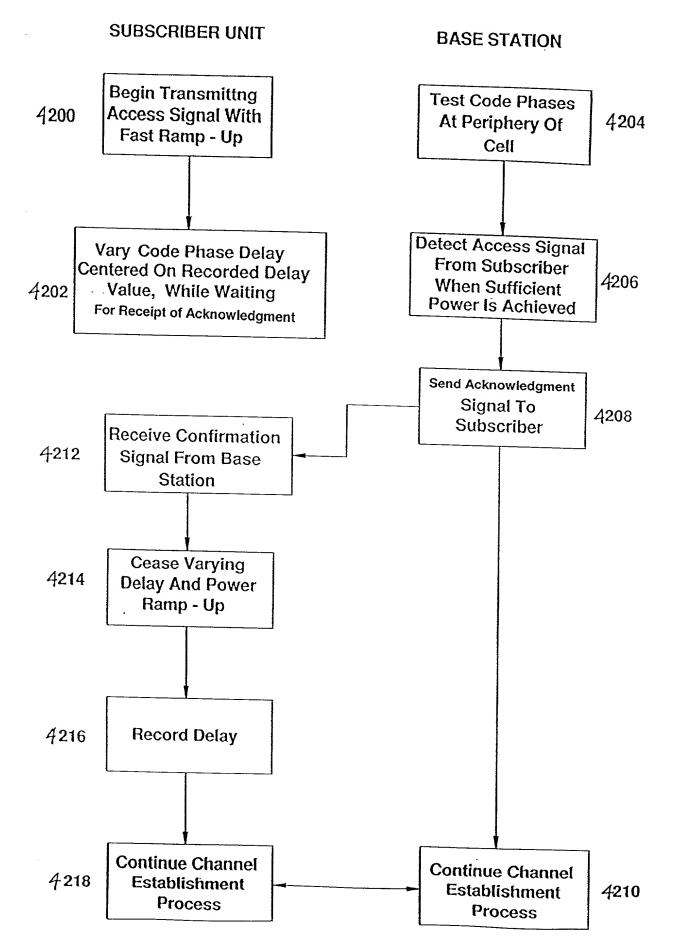


FIG. 47

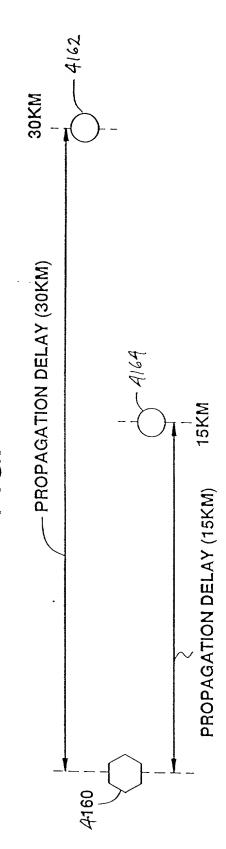
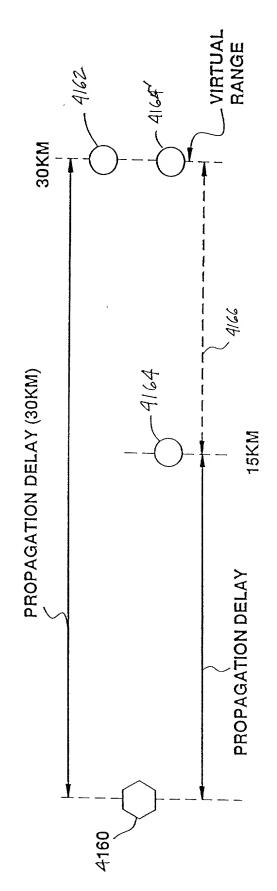


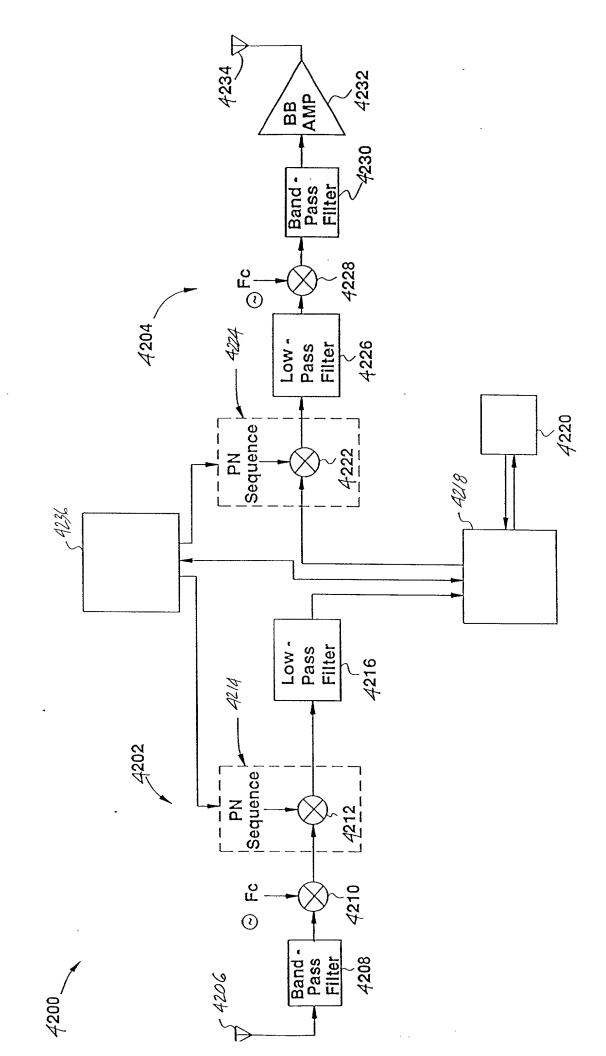
FIG. 48

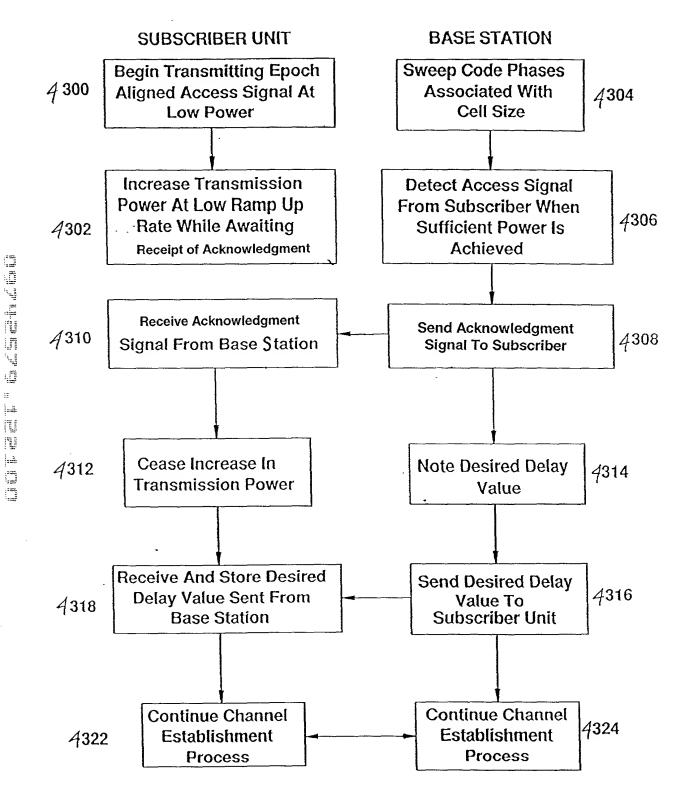


 sU_1 su, SU_2^{-1} -4175 su, SU, SU_2 'BS ຽດຶ su, Su ຣບູ ະກຣ SU₄ ຣິບຸ SU,¹

FIG. 49

FIG. 50





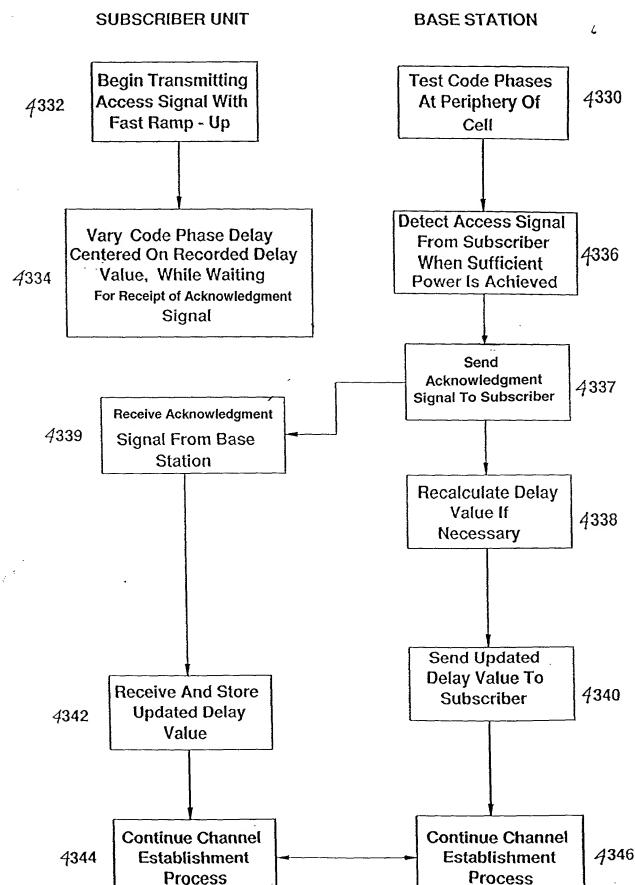
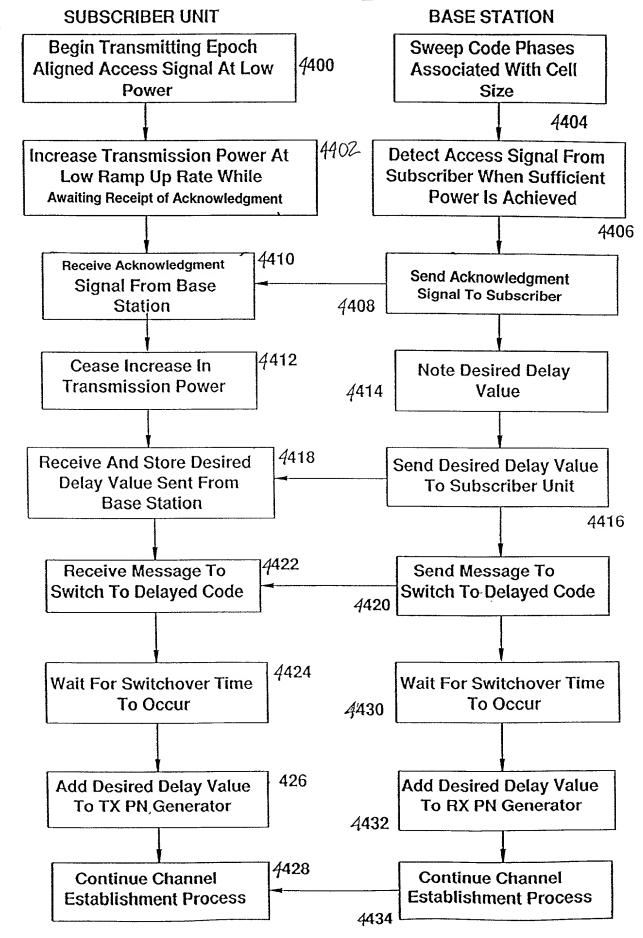


FIG.53



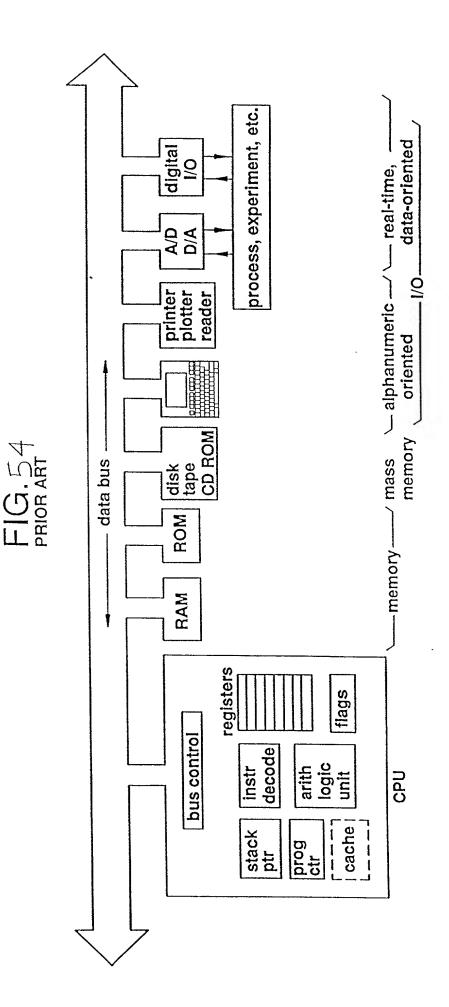


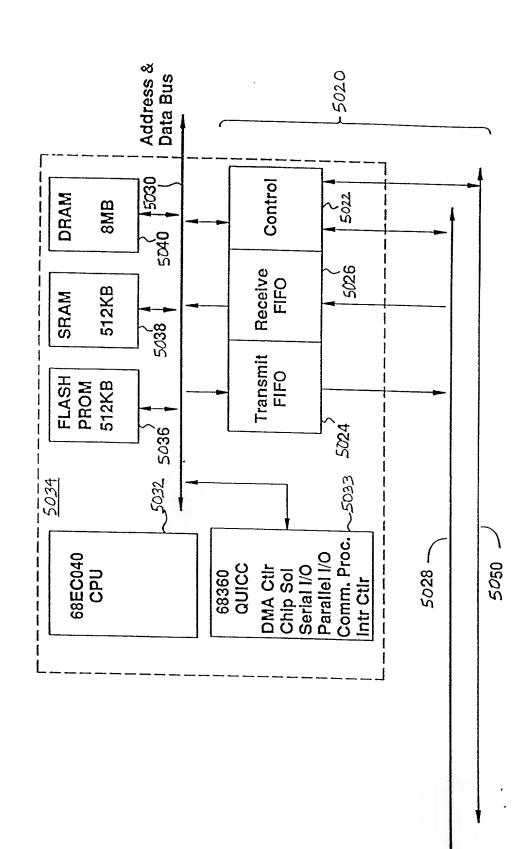
 FIG . 55

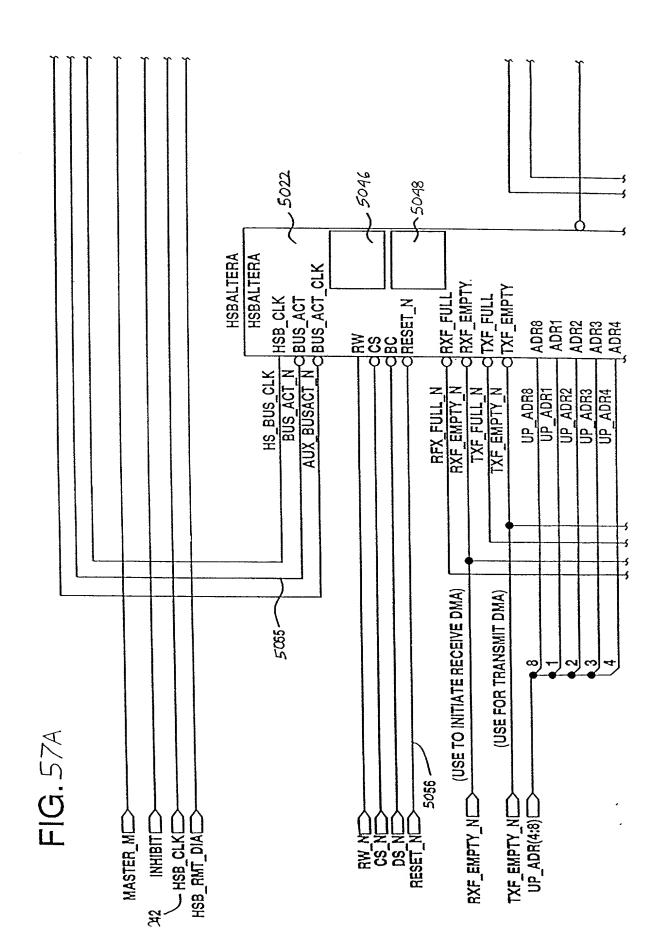
Comments	controller-type applications	original IBM PC & compatibles	accepts PC/XT cards	enhanced PC/AT; auto-configure	IBM PS/2; auto-configure	LSI-11, µVAX-I,II;daisy-chained IACK	Intel; SUN-I and others	data acqusition & control bus	VAX 780, 8600 series; parity	parity; 40MB/s for blk xfer, 20M otherwise	Macintosh II adds 1 dedicated INT per slot; ""	daisy-chained IACK; SUN-3	communication across many crates
Connector b	CE	S	CE	띵	И	S E		S	ZIF	N D	NI D	O N	I
Drivers	I	Ĕ	Ë	Ë	Ë	©	É	TL/OC	F	E	Ħ	Ħ	(d)
IRQ Lines a	Ψ-	5日	10E	11P	1	4	ω		4	Σ	Σ	7	IΣ
Sync/Async	လ	တ	S	ഗ	4	٧	٧	ဟ	တ	ഗ	S	4	44
Multimaster?	1	1	<u>ပ</u>	•	•	•	•	1	•	•	•	•	• •
MUXed data/adr?	1	1	1	1	I	•	1	١	•	•	•	1	•
Block xfer?	1	1	1	•	•	•	1	•	•	•	•	•	•
Address width	16	70	20,24	20,24,32	24,(32)	22	20,24	တ	32	16,32	32	16,24,32	32
n Data width	8	∞	8,16	8,16,32	8,16,(32)		8,16	24	3,16,24,32	3,16,24,32	35	8.16.32	35
RAW bandwidth (Mbyte/s)		1.2	ر ر	33	20	N	9	က	က္	유	9	유	80 80
BUS	STD bus	PC/XT	PC/AT	EISA	MicroChan	Sud - C	Multibus	CAMAC	VAXBI	Multibus II	NiiBiis	VME	Futurebus 1 Fastbus 1

(a) E-edge-sensitive; L-LAM ("look at me"); M-"int" via bus mastership; P-programmable edge-or level-sensitive interrupts.

(b) CE-card-edge; DIN-2-part "Eurocard" 96-pin connector; H-high density 2-part conn. (c) almost. (d) National Semi special.

FIG. 56





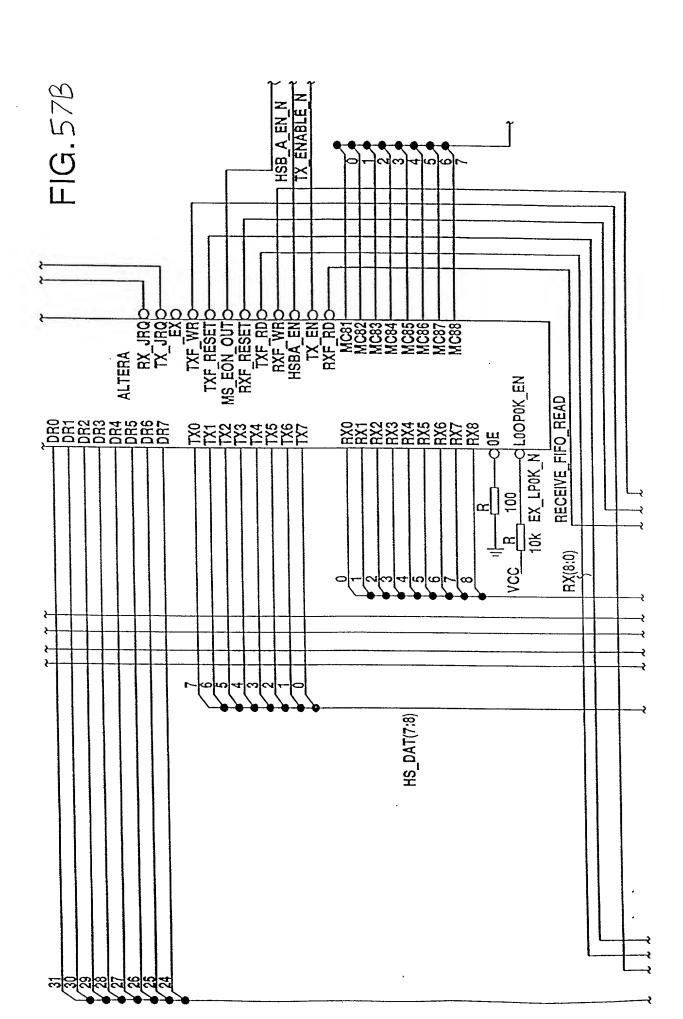
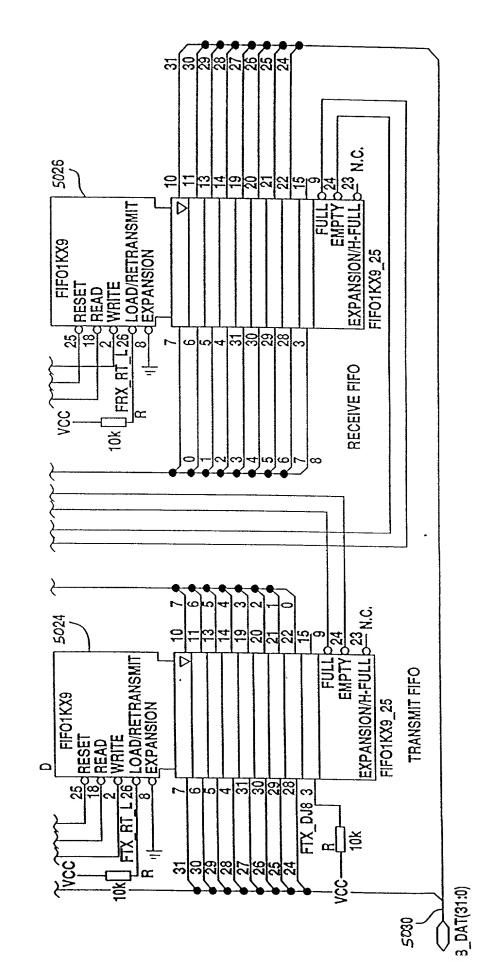
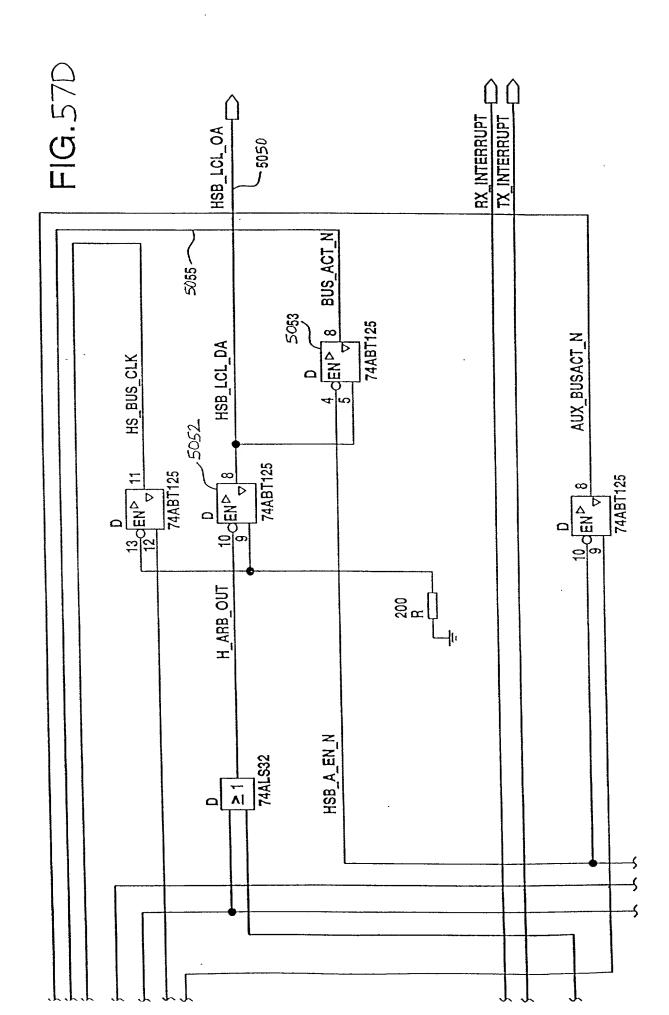
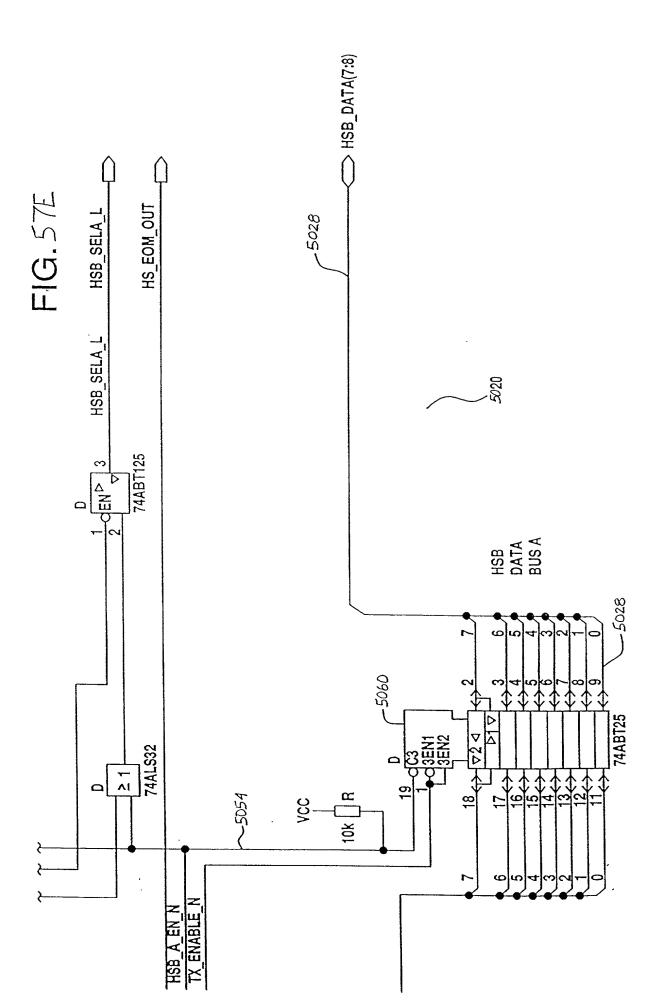
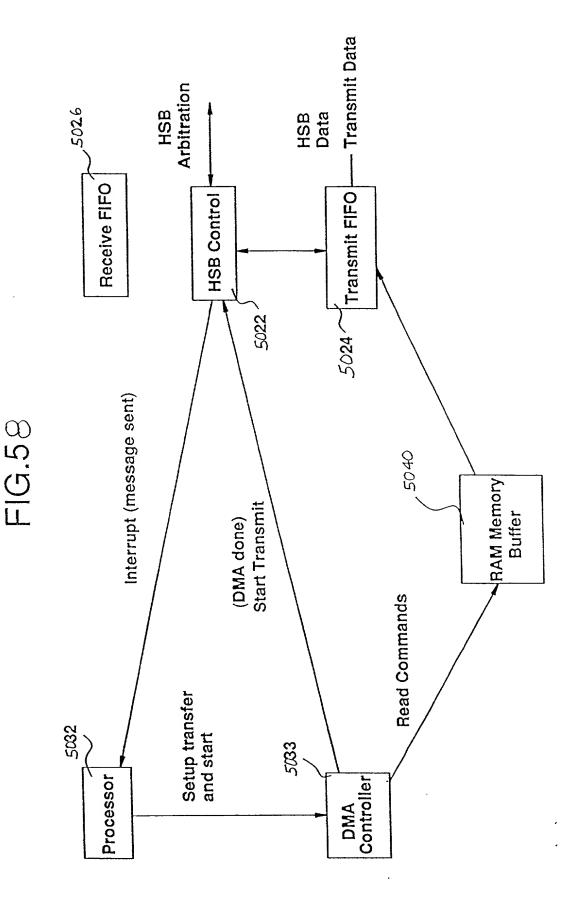


FIG.57C









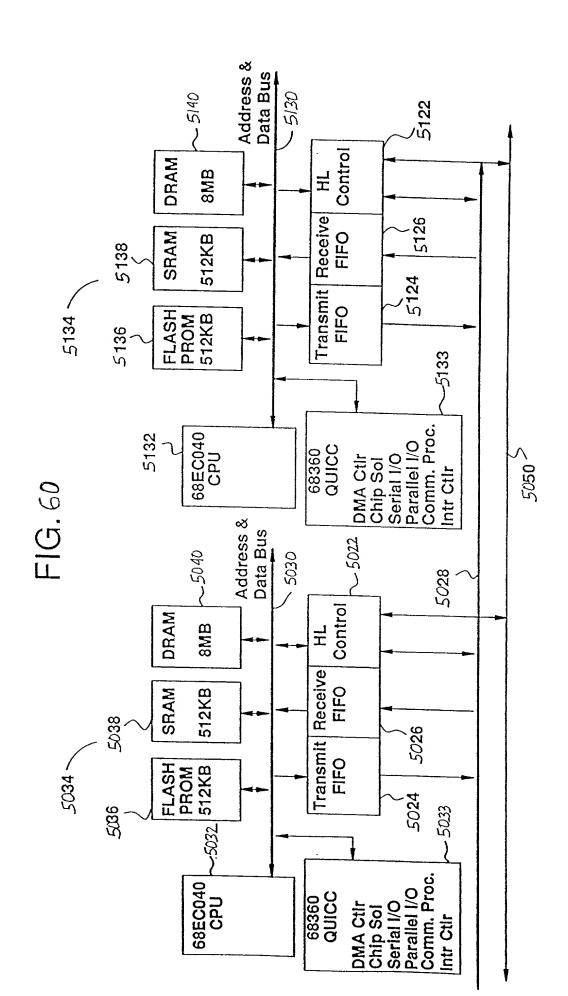
Receive Message Data **HSB** Data Receive FIFO 5024 **HSB** Control Transmit FiFO 5026 5022 Receive Message Data RAM Memory Request Service Done - End Of Message Write Commands Setup DMA Controller Processor 5032 Message Received Interrupt

~5040

Buffer N

Buffer 1 Buffer 2 Buffer 3

FIG. 59



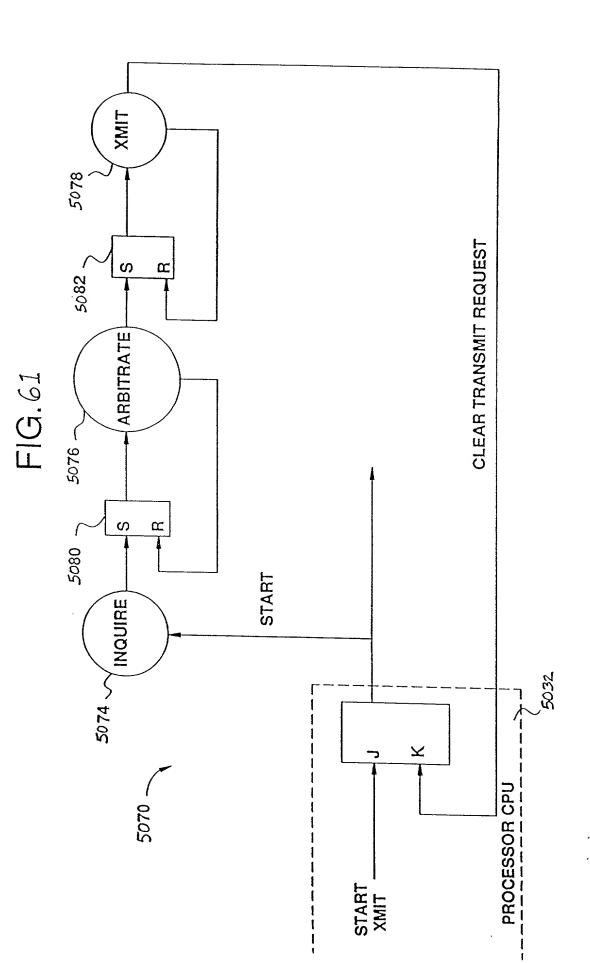


FIG. 62

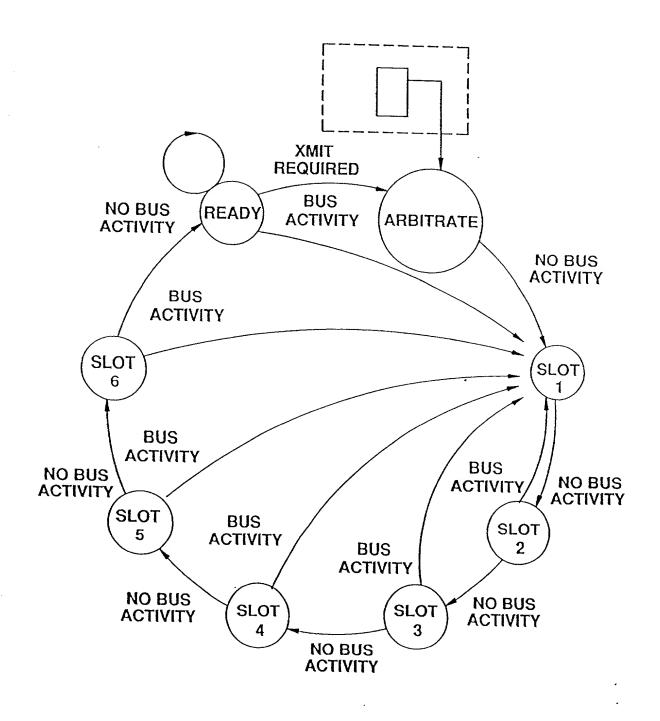


FIG. 63

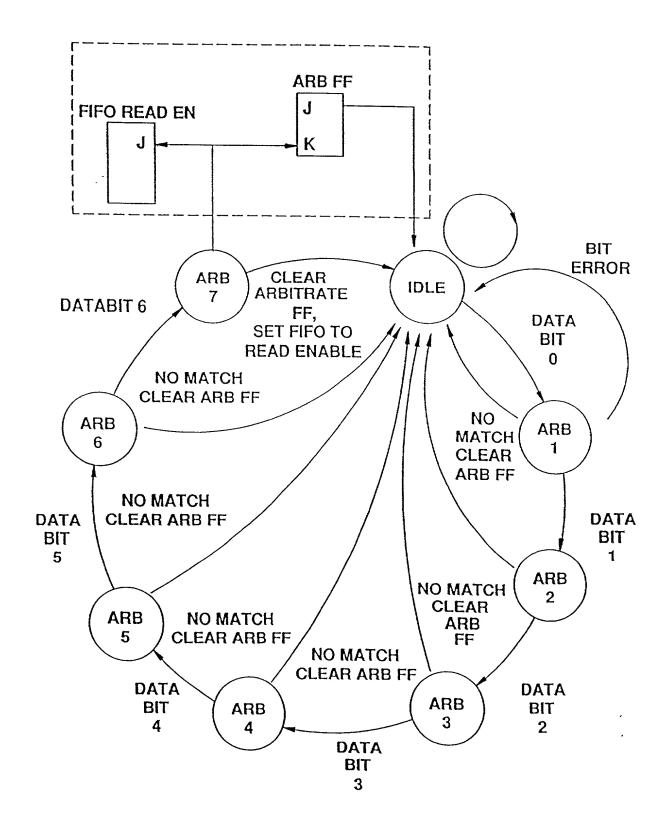


FIG. 64

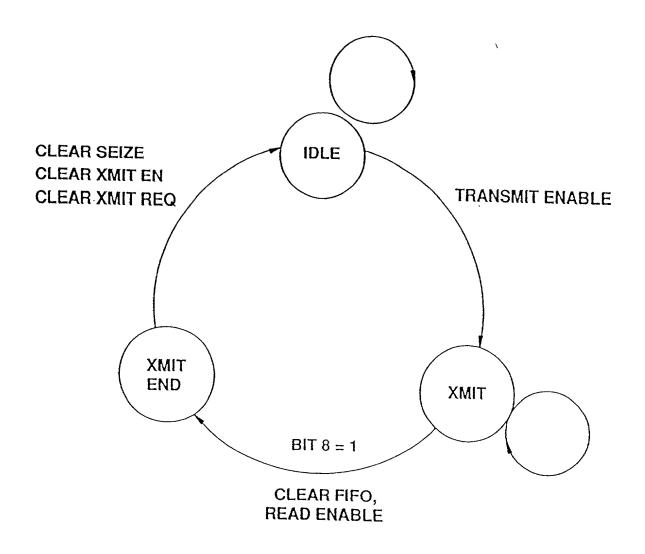


FIG. 65

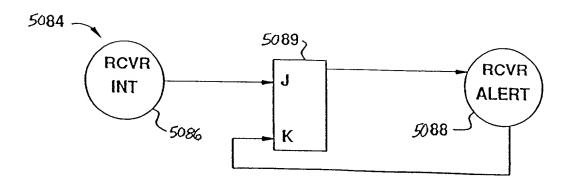


FIG.66

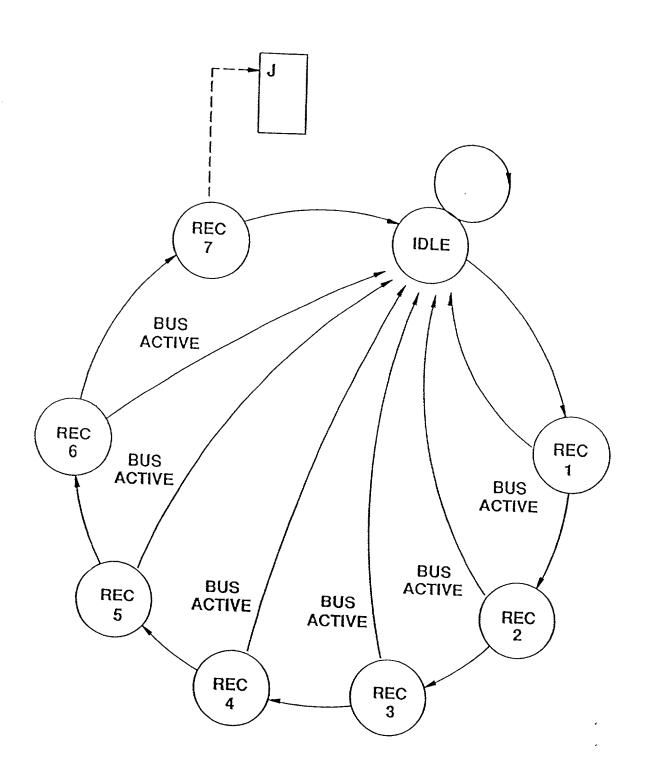
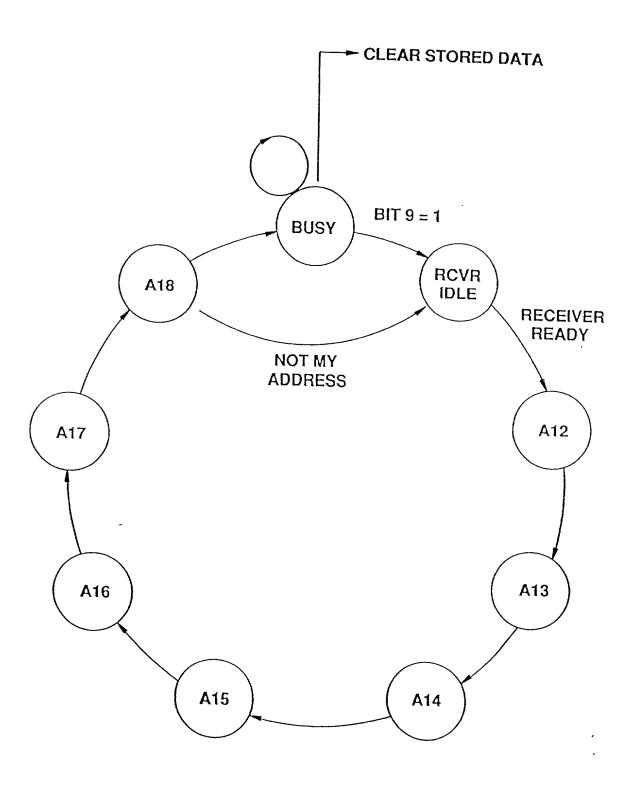


FIG. 67



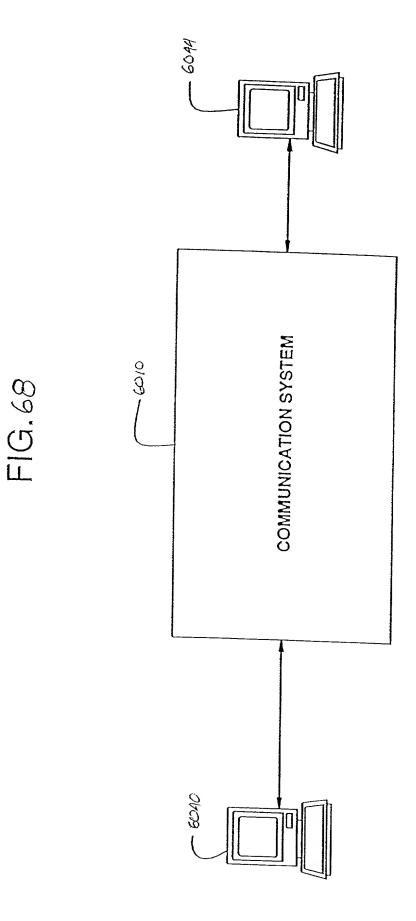
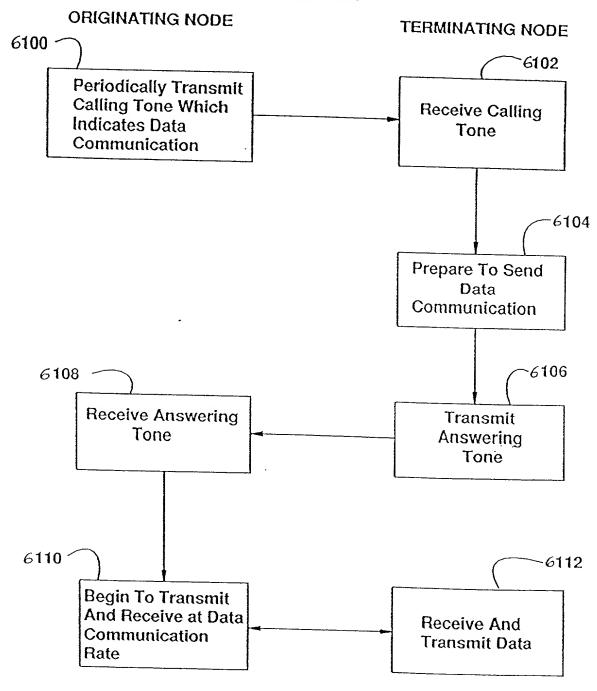


FIG. 69
PRIOR ART



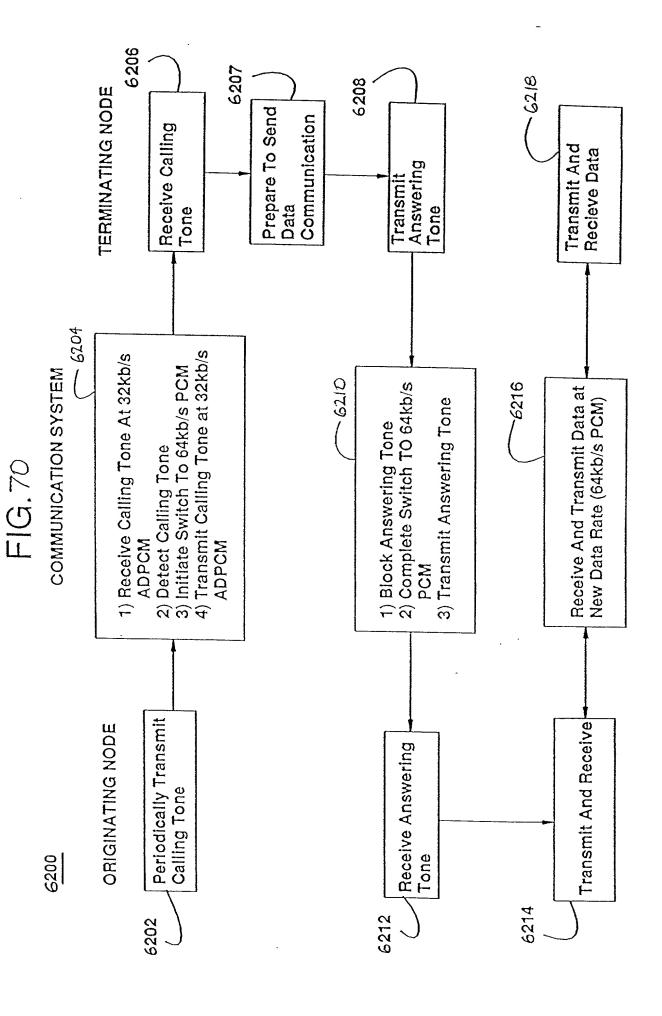
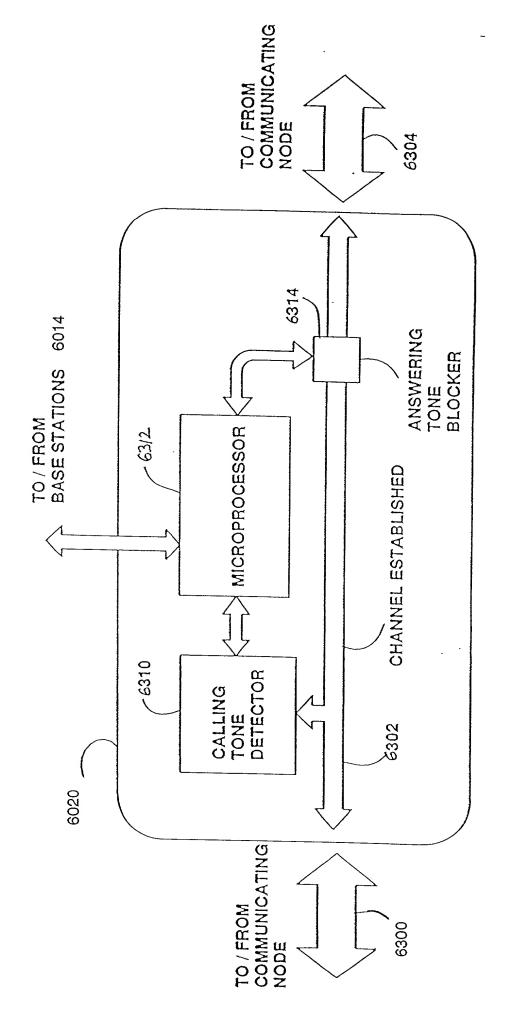
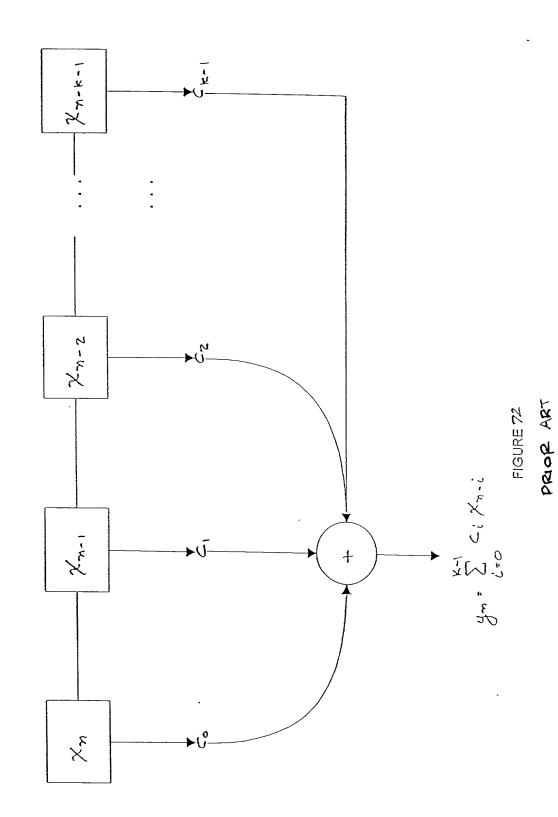
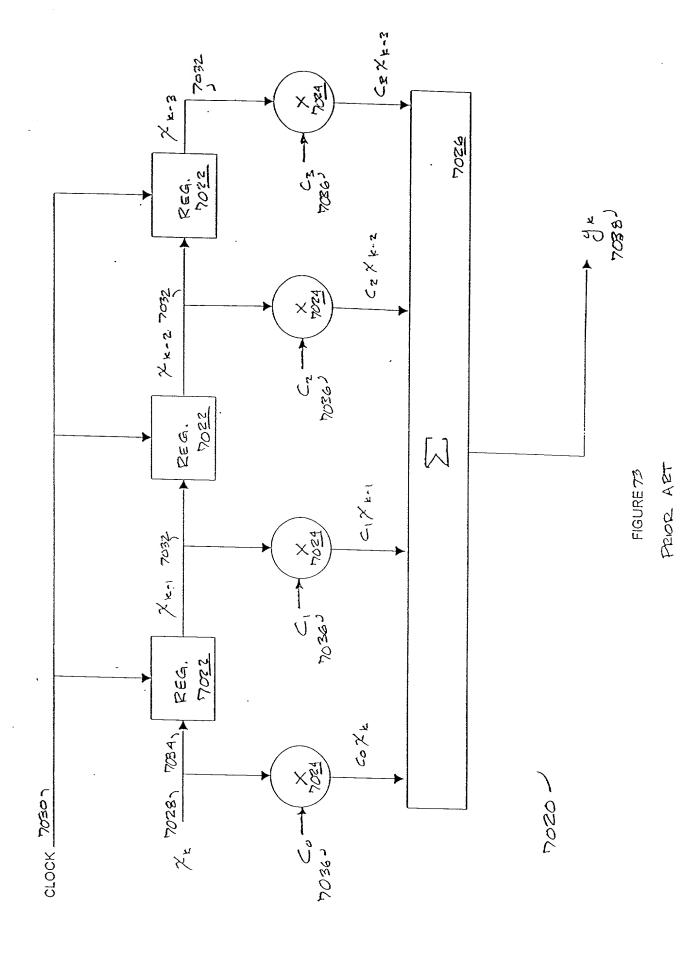


FIG. 71



7020-





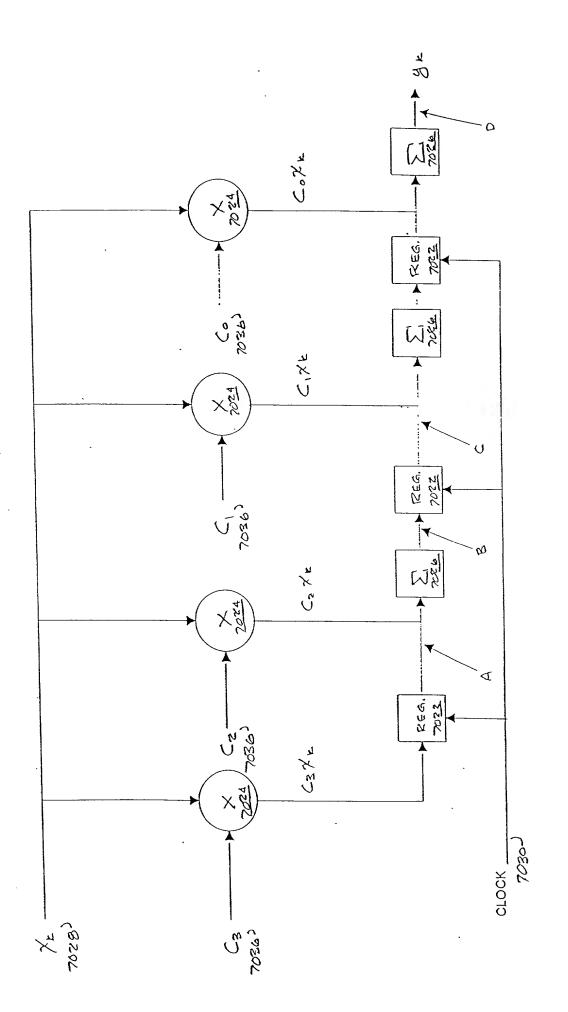
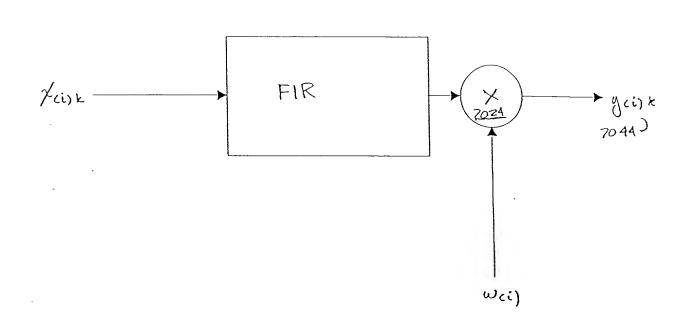
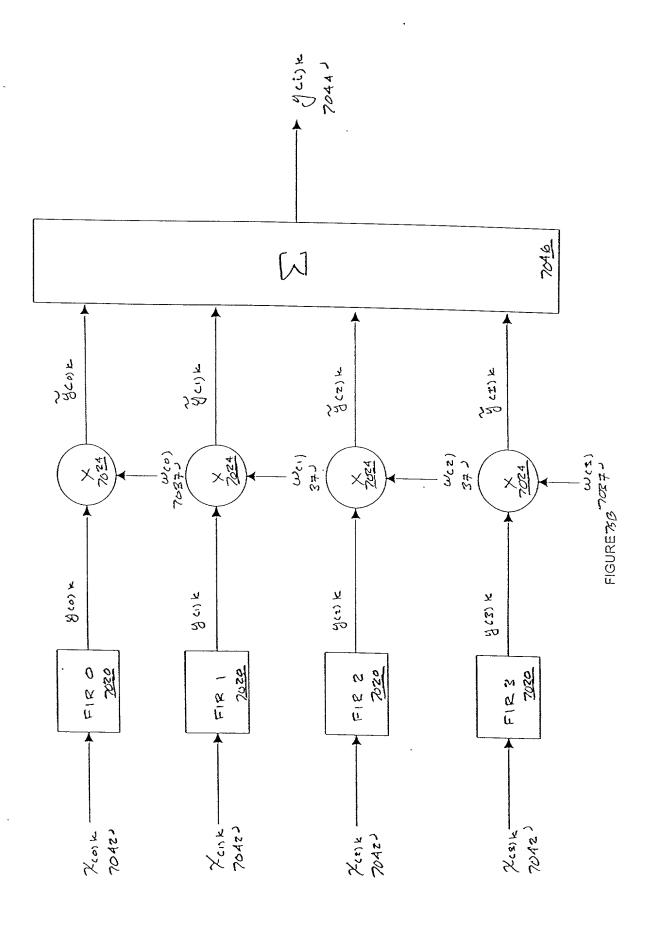
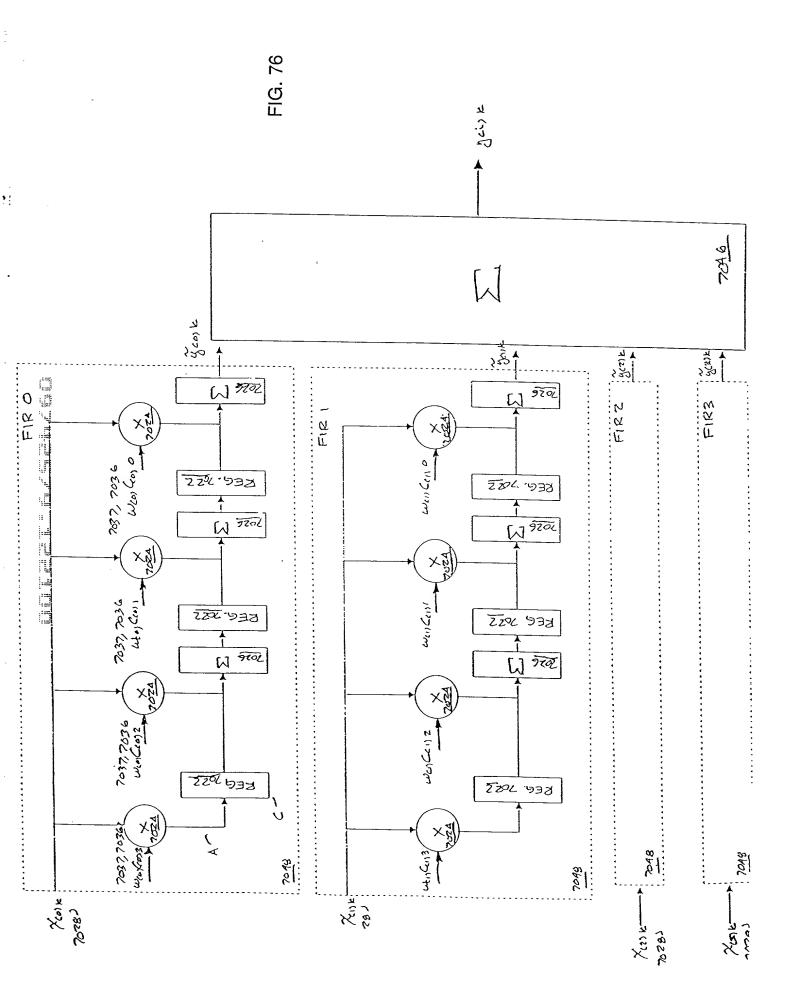


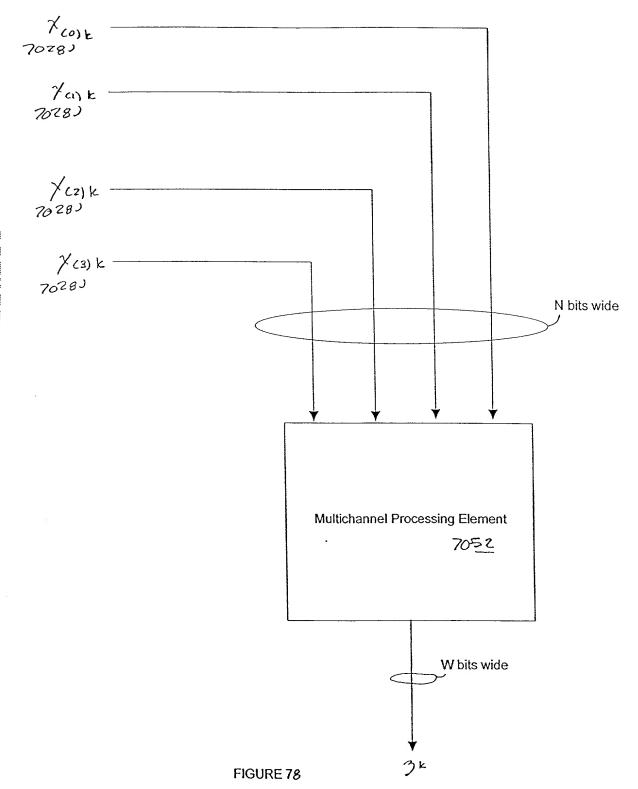
FIGURE 74 PENCA ART

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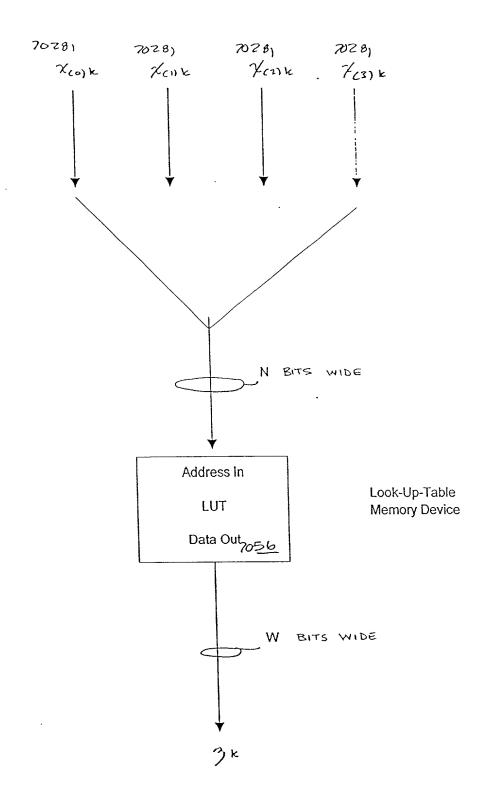


FIGURE 794

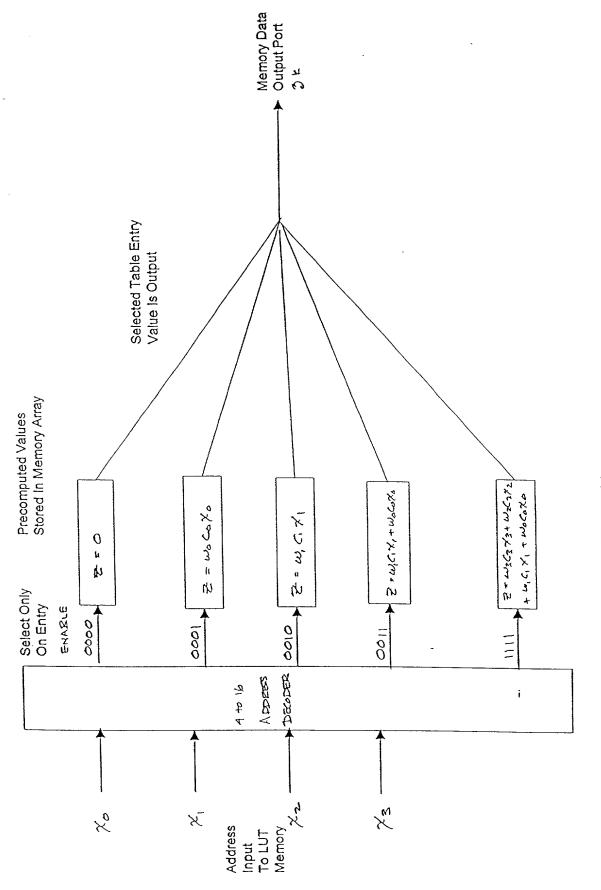


FIGURE 79B

FIGURE 80